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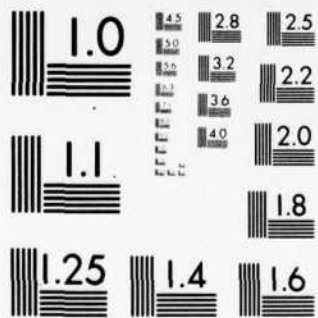
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## ANALOG BUILDING BLOCKS FOR COMMUNICATIONS MODEMS

*ELECTRONIC COMMUNICATIONS INC.  
A SUBSIDIARY OF NCR  
P.O. BOX 12248  
ST. PETERSBURG, FLORIDA 33733*

JANUARY 1977

TECHNICAL REPORT AFAL-TR-76-29  
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Modules delivered included a set of five 70 MHz amplifiers, each with specified gain and bandwidth, a phase-lock frequency multiplier at 4 MHz, and a frequency agile synthesizer with output center frequency in the lower VHF radio spectrum.

Included in the study are discussions of the general requirements for each of the four modules as well as test and evaluation of the delivered units.

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## INTRODUCTION

The enclosed report is for supportive data and information for a series of modules and designs that were produced as a result of a modem partitioning study by AFAL. This study generated a requirement for a series of modules. Each module was identified by the study as a basic functional unit in a majority of modem applications. The modules were translated into a hardware and documentation requirement. This report represents the documentation requirement by providing technical support for design work accomplished. Specific modem areas covered in this report are synthesizers, r.f. amplifiers, multipliers, and demodulators. In each case a piece of hardware was designed and delivered except for the demodulator (Costas Loop) which was a paper study. The synthesizer required a reference generator and information on this module is included in this report.

Each area of the report is written as a complete entity. The specification called for consideration of general requirements as well as hardware items to meet specific requirements. Each major section of the report is organized so that the general requirements are discussed, followed by analysis of the specific requirements. In each case the general requirements examined items like the r.f. amplifiers over a moderately broad range while the specific requirements dealt with one specific frequency, i.e. 70 MHz. The range of consideration for each item in the general case was a function of the statement

of work requirements.

Sufficient information is given in each section so that a thorough understanding of circuit operation, problem areas, and characteristics can be obtained. Also information is provided to allow modification of the hardware for other requirements and frequencies of operation. The Costas study is tutorial in approach to provide basic knowledge for understanding the overall approach.

## SECTION I MULTIPLIER

### 1.1 GENERAL CASE

In many modem applications, it is necessary to perform frequency multiplication from a stable reference source. The desired multiplication ratio may vary from two to many thousands. When this ratio is large, or a prime number, or combinations thereof, conventional frequency multipliers are unacceptable. The primary disadvantage of conventional multipliers is the complexity required to preserve spectral purity, reducing the levels of spurious frequencies at the output. Often crystal lattice filters are required to preserve purity. A more cost-effective solution in these and other complex cases is the phase locked frequency multiplier.

The phase locked loop (PLL) performs frequency multiplication when configured as shown in Figure 1. The frequency divider ( $\div N$ ) is the multiplication ratio between the input and output frequencies. A phase error ( $\theta_e$ ) exists between the VCO and the reference signal. A control signal, generated by the phase detector, proportional to the phase error, locks the VCO to the proper frequency. The loop filter controls the closed loop bandwidth of the PLL.

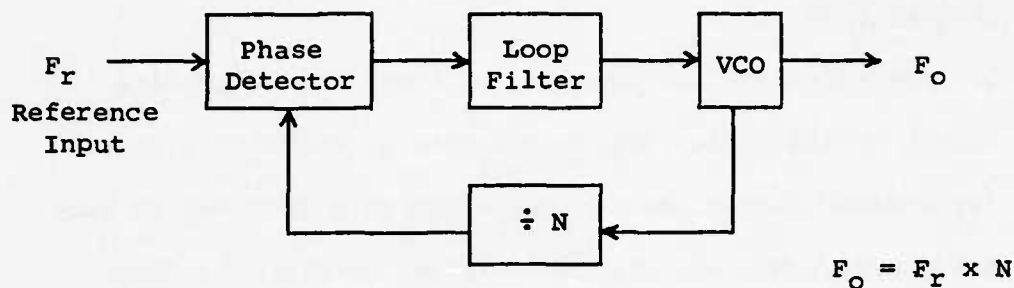


Figure 1. Phase Locked Frequency Multiplier

Spectral Purity (SSB in one Hz BW)

The specification defines the phase noise as associated with the output signal. In any frequency multiplier signals of  $(N-2)$ ,  $(N-1)$ ,  $(N+1)$ ,  $(N+2)$ , etc., times the input frequency appear at the output. For example, the four MHz unit has a factor of  $\frac{4 \times 10^6}{100 \times 10^3}$ , or 40. Signals at 38, 39, 41, and 42, etc., appear at the output. The attenuation to these and all other undesired outputs is determined by the bandpass filtering included in the signal path. This is also true for the phase locked multiplier. The required bandpass filtering takes the form of a lowpass filter at baseband, translated to RF (4 MHz) as the bandpass equivalent. The resultant selectivity is determined by the PLL design. The most severe constraint in the PLL is the

tradeoff between reference sideband rejection (requiring narrow loop BW) and low phase noise (requiring wide loop BW).

The problem becomes critical as the reference frequency is lowered. The output of the PLL multiplier with a 10 to 50 KHz reference contains spurious sidebands within the range specified for spectral purity. Attenuating these sidebands 100 dB to 120 dB below the carrier is a formidable task. Attenuation of phase noise, however, to these levels is within the state-of-the-art. Therefore, ECI recommends that AFAL give special consideration to the specification of low reference frequencies within the range where phase noise spectra is critical to the equipment usage.

#### Voltage Controlled Oscillator

The voltage controlled oscillator is a critical building block in the phase locked multiplier. The VCO accepts the error signal from the phase detector changing frequency until the VCO becomes phase coherent with the reference frequency. The spectral purity of the VCO attains that of the reference standard (times the multiplication factor) because of the tracking exhibited by the closed loop. As tracking or "clean up" occurs within the loop bandwidth, the VCO noise is reduced. Outside the loop bandwidth no tracking occurs; the resulting noise spectrum is determined

solely by the VCO.

The noise characteristics for this family of multipliers are specified as: (SSB C/N per Hz)

f	dB/Hz
200 Hz	-20 dB
2.0 KHz	-80 dB
50 KHz	-120 dB

#### Oscillation Criteria

The simple feedback system shown in Figure 2 provides the necessary criteria for self-sustained oscillations. That is, at  $f_0$  the signal fed back to the input is sufficient in magnitude and proper phase to act in an additive nature with the signal initially present. Build up occurs (starting with thermal noise) until amplitude limiting stabilizes the output signal. The frequency selective network (such as an L-C resonant circuit or crystal device) determines the frequency of oscillation by providing a varying phase shift in the loop. Frequency is automatically adjusted until the exact phase angle is attained.

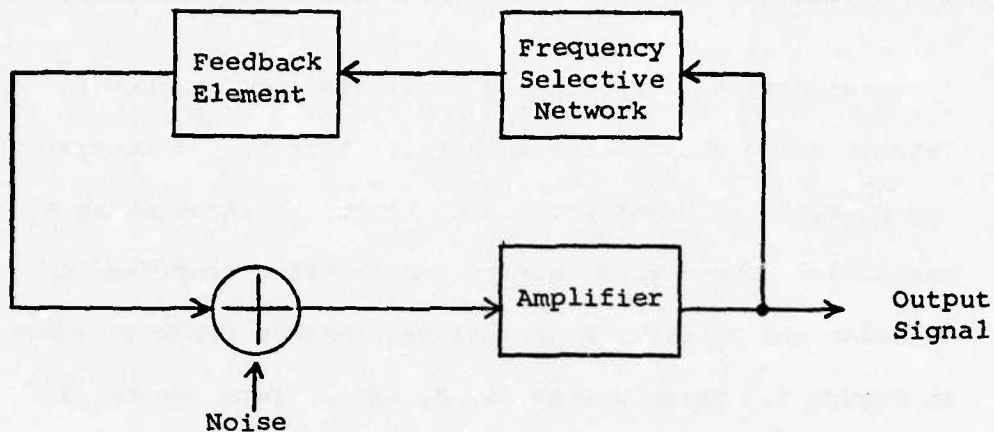


Figure 2. Simple Oscillator Feedback System

#### Noise Criteria

All oscillators develop incidental frequency modulation (IFM) because noise is injected into the loop. Although noise sources are distributed in location, a single injection point may be assumed at the amplifier input. The dominant effect is that the noise is interpreted by the loop as a phase error, i.e., a departure from zero degrees phase shift around the loop. To re-establish zero degrees, frequency of oscillation shifts enough for the resonator to develop a voltage equal but opposite to the injected noise. Thus, the injected noise is nulled out, but the oscillator has been frequency modulated by the noise. The amount of frequency shift is inversely proportional to the loaded  $Q$  of the resonant circuit and directly proportional to the magnitude of

the injected noise (noise factor of the active device).

A useful method of specifying oscillator performance is "single sided phase noise spectra." This data illustrates the phase noise power per one Hz bandwidth existing at a particular offset from carrier and is often specified in dB below the carrier. A general performance curve is shown in Figure 3. Three curves (A, B, and C) form the total phase noise characteristic. At frequencies below  $f_1$ , flicker noise becomes dominant (Curve A) as expected because of the associated  $1/f$  power spectra. At frequencies greater than  $f_2$ , thermal noise floor dominates the spectra (Curve C). Frequency  $f_2$  is determined by the bandwidth of the resonant circuit in the feedback path. Curve B is the phase modulation spectrum resulting from constant fm deviation (by noise) within the resonator bandwidth.

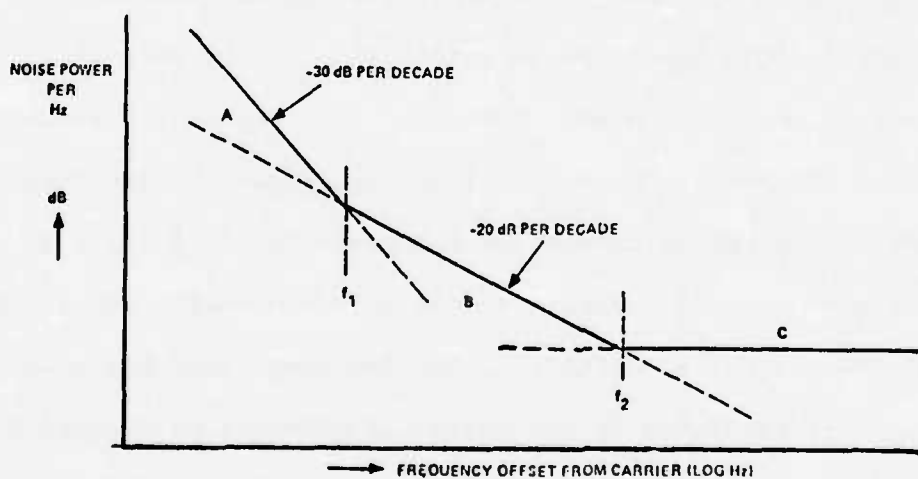


Figure 3. Single Sided Phase Noise Spectra (General Curve)

An equation is proposed without derivation here that characterizes this noise spectra. Exact correlation between the theoretical and results achieved is somewhat difficult because of the inaccuracies in the prediction of oscillator parameters (such as flicker noise, noise figure, and loaded Q), once oscillation occurs.

$$L = \left[ \left( \frac{3000}{f} + 1 \right) 2 \left( \frac{f_0}{2Q} \right)^2 + 1 \right] \frac{KTF}{2P_{in}}$$

Where:

- L = Single sided phase noise per one Hz BW measured in power relative to the carrier
- KT = Thermal noise power at room temperature (-174 dBm)
- P<sub>in</sub> = Power feedback appearing at the input port of the oscillator
- F = Noise factor of the active device while oscillating
- f = Frequency of interest, Hz removed from the carrier
- f<sub>0</sub> = Frequency of oscillation
- Q = Loaded Q factor of the resonator

The term  $\frac{3000}{f}$  accounts for flicker noise, assured to dominate at three KHz. The term  $\frac{f_0}{2Q}$  accounts for frequency deviation within the resonator bandwidth, division by 2f accounts for single sided, and phase modulation conversions.

The modifier,  $\frac{KTF}{2 P_{in}}$ , controls noise performance of the oscillator as expected. This term relates the signal to noise factor at which the oscillator is operating. It is

appropriate now to analyze an L-C oscillator design with this format and compare the results with the multiplier specifications listed previously. The following parameters are analyzed:

$$f_o = 120 \text{ MHz}$$

$$Q = 50$$

$$P_{in} = 1 \text{ milliwatt}$$

then,

$$\frac{KTF}{2 P_{in}} = -168 \text{ dB/Carrier}$$

and at  $f = 50 \text{ KHz}$

$$L \cong \frac{KTF}{2 P_{in}} \left[ 2 \left( \frac{f_o}{4 QF} \right)^2 \right]$$

$$L \rightarrow -144 \text{ dB/Carrier}$$

These points and others are shown graphically in Figure 4.

The noise spectrum calculated exceeds AFAL's requirements. In practice, the L-C oscillator performance is deteriorated because it must be voltage tuned, possibly with varactors which lower the available  $Q$  and, more important, transfer noise from the phase detector and control circuits directly into incidental frequency modulation. The 20 dB of noise margin illustrated in the L-C oscillator quickly diminishes.

The PLL will attenuate the low frequency portion of the noise curve; the trend is to force the VCO to attain the very low noise characteristics of the reference signal. This is

illustrated in Figure 4. A wide loop bandwidth is desired so that the output signal will more closely attain the low noise performance of the reference.

A tradeoff must be made here. The PLL bandwidth is limited because it is a sampled data system. Excessive phase shift occurs as the PLL bandwidth approaches one-half the sample frequency,  $f_s$ . Further, signals at the reference frequency appear in the form of spurious sidebands. These requirements generally limit the loop bandwidth to  $f_r/10$ . For this equipment, the lowest frequency reference is 10 KHz. This implies loop maximum bandwidths in the order of 500 to 1000 Hz. A lowpass L-C filter is included in the control path to attenuate the 10 KHz components.

The PLL bandwidth is large enough so that vibrational and other microphonic perturbations are reduced to a negligible level. Further, spurious phase jitter is reduced to less than two degrees rms. This parameter is most important in systems containing phase modulation, such as PSK and QPSK.

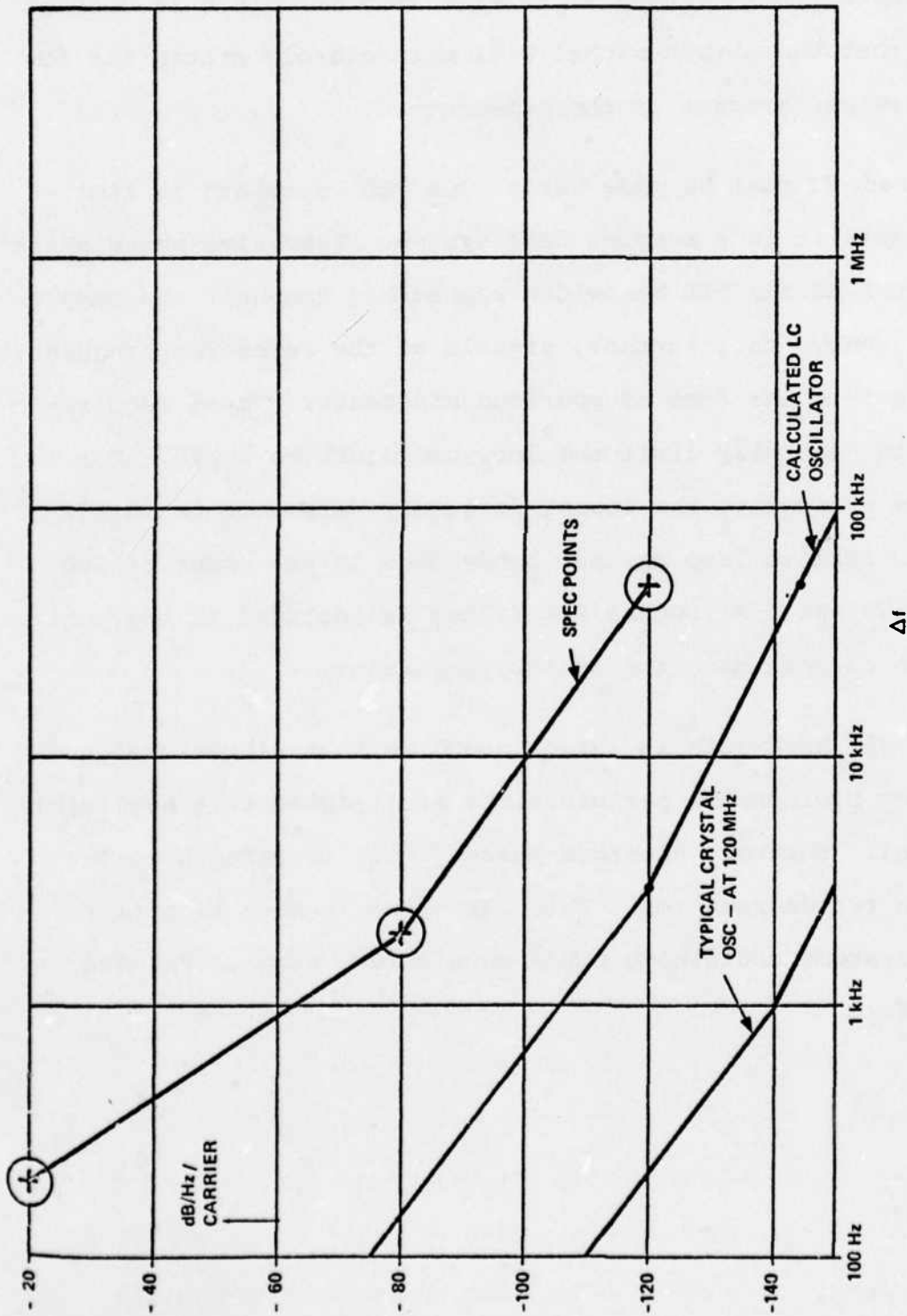


Figure 4. Single Sided Phase Noise Spectra

Returning to the phase lock loop block diagram (Figure 1) it can be seen that the key implement to achieving phase coherence is the phase detector for its output is the actual controlled variable. The VCO output is related to it through the loop filter and VCO circuitry. Typically, the phase detector operates at the frequency of the input signal. Multiplier output frequency is divided by a modulo N counter whose output is at the phase detector frequency. This scheme assumes that the phase detector will operate at any input frequency and the modulo N counter will operate at any multiplier output frequency. This, however, is not always the case.

Building the appropriate phase detector at any radio frequency is a problem but the modulo N counter is more of a problem. With increasing frequency, the type of counter changes and each type has its particular tradeoff. We may have to trade any combination of programmability, modulus N value, power consumption, complexity and cost for counting speed. The most serious tradeoff is the value of modulus N available since it tends to challenge the very design feasibility. There are ways around this, however, such as prescaling the output frequency before dividing by N and also prescaling the input frequency. Doing this, however, also has its tradeoffs.

Multiplying any frequency in the 10KHz to 1MHz range to any integral multiple in the 20KHz to 120MHz range is the most general statement of the task at hand. A single piece of equipment, which would accomplish that, would, indeed, be complex and expensive. It is thus understood that constraining certain parameters would be a more realistic approach.

#### 1.1.1 Advantages and Limitations

Since the output frequency places a burden upon the N counter, it is convenient to partition into ranges of output frequency. Important also are the limitations on counting modules, N, within each output frequency range. In addition, the frequency of the phase detector must be included as this has an effect upon the overall input to output multiplication ratio.

The phase detector presents a problem when an input frequency range is specified rather than a single value. If the phase detector operates at the input frequency then it has to be capable of operating either over a large range (10KHz - 1MHz) or of being mode switched to accommodate much smaller ranges of input frequency.

Another option is for the phase detector to operate over a large frequency range but at some subdivision of the input frequency to compensate for prescaling the VCO output frequency.

A third option would be to operate the phase detector over a small range (say 10 KHz to 20 KHz) irrespective of what the input frequency is. Although this simplifies the phase detector design it is awkward when the input frequency is very high and thus presents its own problems.

The schemes presented shall then be partitioned into frequency ranges as follows: Output Frequency,  $f_o \leq 10$  MHz;  $10 \text{ MHz} \leq f_o \leq 40$  MHz;  $40 \text{ MHz} \leq f_o \leq 80$  MHz; and  $80 \text{ MHz} \leq f_o \leq 120$  MHz.

#### 1.1.2

##### Block Diagrams

Except where otherwise indicated, the following cases assume that:

- (a) The phase detector will operate at whatever the input frequency is.
- (b) The VCO will operate at the indicated output range.
- (c) The counter's modulus,  $N$ , can be changed through switching or simple rewiring.

##### CASE I - $f_o \leq 10$ MHz, Figure 5

If the output frequency is less than 10 MHz the counting can be done by a standard TTL programmable counter. To accommodate the largest division ratio,  $N = 1000$ , three decade counters must be used. Propagation and setup delays are not yet a large part of the period of the input signal and thus do not hinder counter operation. The phase detector operates

If  $f_o \leq 10 \text{ MHz}$ :

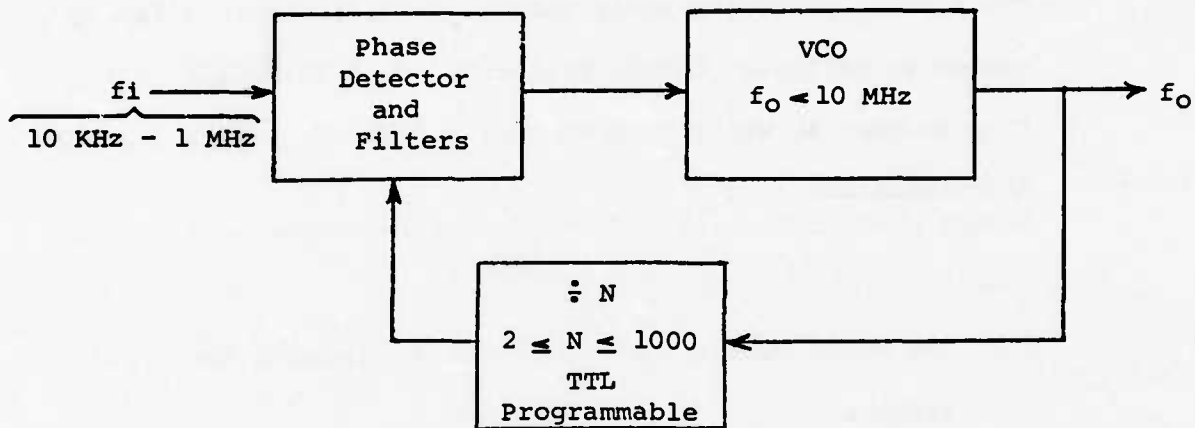


Figure 5. Case I, Block Diagram

over the given input frequency range (some other frequency determined by an appropriate choice of M, an input divider, could be used for input frequencies near 1 MHz. Note that to compensate for the input divider, M, modulus N would have to be multiplied by M.)

When the output frequency is in the kilohertz range difficulties are encountered in building the VCO. The values of inductance and capacitance required become very large from an RF standpoint. The inductor in particular, becomes physically large and mounting becomes a problem especially where vibration is present. Capacitance is a problem because of the need for voltage tuning. Tuning varactors above 100 pf in value are relatively rare. Moreover, as the capacitance increases the value of Q decreases. This is in direct conflict with low noise requirements. As a result, to obtain an output frequency up to 3 MHz, the VCO should be built at a frequency above 3 MHz and divided down with digital counters. Where a sinewave is required tuned circuits will have to be used.

CASE II -  $10 \text{ MHz} \leq f_o \leq 40 \text{ MHz}$ , Figure 6

When the multiplier's output frequency exceeds 10 MHz propagation and setup delays prevent reliable counting. The counter must recognize that it has performed N counts, reset itself to zero, and be setup to count to N again in one

If  $10 \text{ MHz} \leq f_o \leq 40 \text{ MHz}$

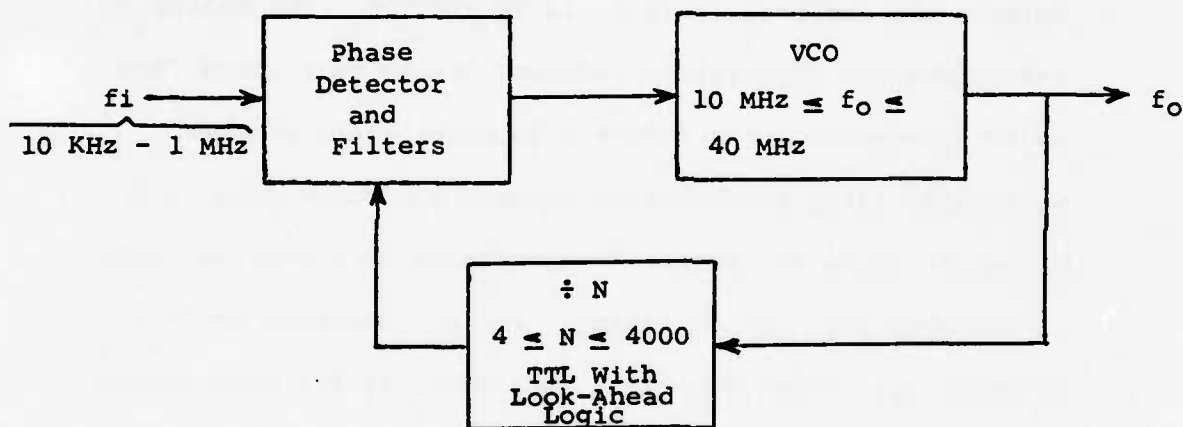


Figure 6. Case II, Block Diagram

counter input signal period minus the propagation and setup delays. When the counter input period shrinks sufficiently it becomes impossible to perform the required operations before the next counter input pulse occurs. To permit counting under these conditions a scheme can be used which allows the counter a few input periods in which to reset. While the counter is resetting an auxiliary fixed modulus counter completes the N count by counting the periods allotted to the reset process. The process by which the reset mechanism anticipates the completed count is called "Look-ahead". This type of counter can operate reliably to 40 MHz using TTL-S logic. It, of course, is more complex, more expensive and larger than the standard programmable counter. However, it does permit counting by any number up to 4000 in this case. (NOTE: Very small numbers such as 2, 3, 4 which fall into the domain of the auxiliary counter cannot be counted.)

#### CASE III - 40 MHz $\leq$ fo $\leq$ 80 MHz - Figure 7

To count up to 80 MHz a pulse swallowing counter is used. Pulse swallowing has two fixed dividers at the counter input with a difference in count base of one. Typically, these bases are 10 and 11. The selection of 10 or 11 is achieved by control circuitry programmed by lower speed logic. This technique extends the counter capability by a factor of 10 in speed, that is, 8 MHz counters are controlling 80 MHz circuitry. The operation is that of counting by eleven until

If  $40 \text{ MHz} \leq f_o \leq 80 \text{ MHz}$ :

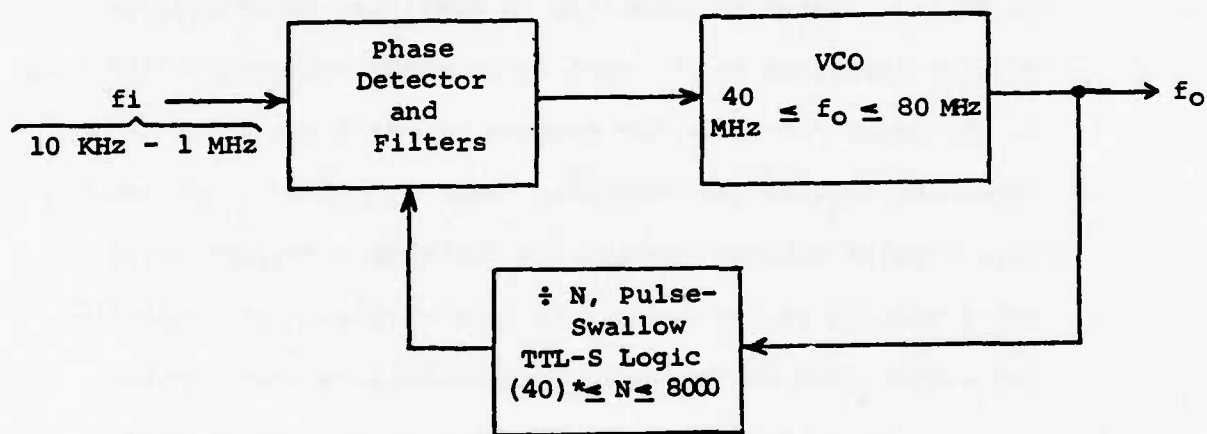


Figure 7. Case III, Block Diagram

the remainder has a zero units digit. The remainder count can then be completed by counting by ten. A consequence of this technique is that numbers below 99 which are not multiples of eleven cannot be counted. In frequency synthesis this is seldom a problem since large moduli are normally encountered. But, in a phase locked multiplier requiring a relatively low modulus it would be restrictive. The multiplier input and output signals whose frequencies fall into this range and are related by such a low multiplication factor could be phase locked only by modifying this basic scheme. At a frequency of about 80 MHz the usual delays inhibit counting in this scheme.

#### CASE IV - $80 \text{ MHz} \leq f_o \leq 120 \text{ MHz}$ - Figure 8

Above 80 MHz the scheme is the same as the previous one but is treated separately because of the type of logic needed. The few nanosecond delays needed to operate in this frequency range can be provided only by using emitter-coupled logic (ECL). Besides the expense, there are other reasons ECL should be used only when necessary. For example, not all ECL is available in the full  $-55$  to  $+125^\circ\text{C}$  military temperature range. Also, whereas a standard TTL gate might consume 10mW of power an ECL gate might consume 70mW. High speed toggling, in general, uses a lot of power. Moreover, ECL does not interface directly with TTL. Separate interface circuitry must be included when mixing ECL and TTL. Some ECL, however,

If  $80 \text{ MHz} \leq f_o \leq 120 \text{ MHz}$ :

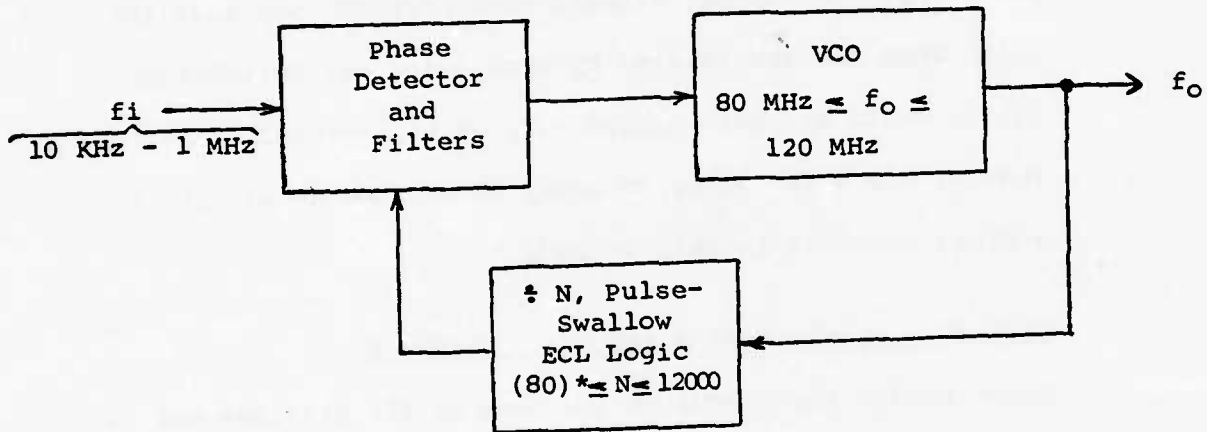


Figure 8. Case IV, Block Diagram

is available with the interface circuitry included in the ECL package. Finally, delivery of ECL logic is not very dependable. It thus behooves one to reconsider a scheme which is dependent for its feasibility upon ECL. Nevertheless, a phase locked multiplier requiring multiplication of the 10 KHz to 1 MHz range by  $N = 99$  to  $N = 12000$  can be realized using emitter coupled logic. As in the previous scheme numbers below 99 cannot be accommodated. A different scheme having concomitant tradeoffs would have to be employed.

#### 1.1.3

##### Recommendations

The four preceding cases demonstrate the general capabilities and limitations of programmable counters as integrated into a phase lock multiplier scheme. As mentioned, there are many ways to configure such a circuit to take best advantage of a capability and to control the effects of a limitation. Since the input and output frequencies are controlling variables a degree of freedom still exists in the selection of the phase detector frequency.

The phase detector does not have to operate at the multiplier input frequency. Consider a multiplier unit in which the phase detector and the VCO frequencies are prescaled by the same factor and the unit can adapt to various input/output frequency requirements by programming counters and through switching within the phase detector. Let the prescaling

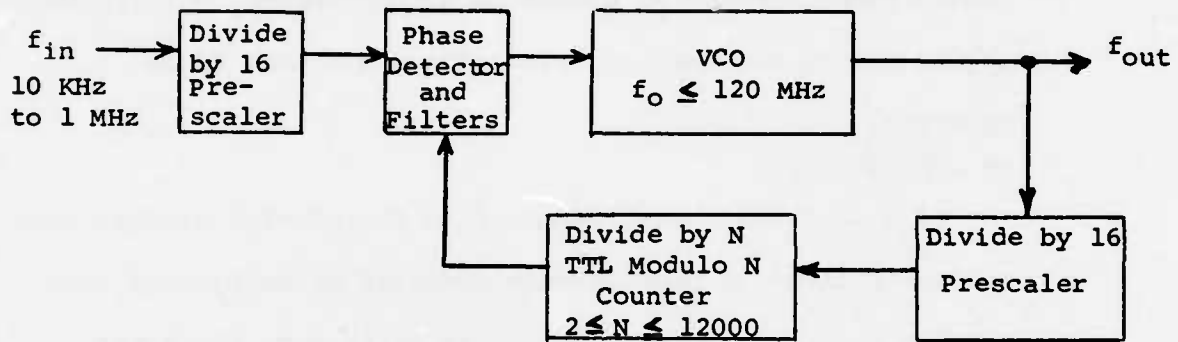


Figure 9. Phase Lock Multiplier Using  
Divide by 16 Prescalers

factor be 16. (See Figure 9).

The highest VCO frequency is 120 MHz so the programmable counter never receives more than 7.5 MHz in which case a standard TTL programmable counter suffices. Thus, all moduli from 2 to 12000 are available. The modification, however, has an impact upon the attainable level of incidental FM. Lowering of the phase detector frequency, in this case as low as 1 KHz, tends to increase the VCO sideband level at the phase detector frequency. Actually, low phase detector frequency contributes doubly to high sideband levels as will now be shown.

First, the FM sideband levels, relative to a unity carrier, are equal to  $\frac{1}{2}$  the modulation index,  $\frac{1}{2} \beta$ , which equals  $\frac{1}{2}(\Delta f/f_m)$ . ( $\Delta f$  is the perturbation of the VCO due to the phase detector). Therefore, for a given  $\Delta f$  the sidebands will increase with decreasing rate,  $f_m$ ; where  $f_m$  is equal to the phase detector frequency.

Second, a filter (other than the loop compensation filter) is always placed between the phase detector and the VCO to attenuate phase detector energy at the VCO. In order to not interfere with the loop tracking characteristic, this filter must begin its roll-off a few octaves above the loop bandwidth. The phase detector frequency should be at least a few octaves above the filter's roll-off of the filter to

have an adequate effect. If the phase detector frequency is low it will not be far enough above the filter's roll-off to be sufficiently attenuated.

When the input frequency is high (1 MHz) no problem exists since prescaling by ten (10) yields a fairly high phase detector frequency of 100 KHz. The worst case exists when a 10 KHz input signal is prescaled by ten (10) down to a 1 KHz phase detector frequency.

It should also be noted that phase detector frequencies below 50 KHz would cause sidebands that fall into the range for which phase noise has been specified. The presence of such sidebands could easily nullify the effect of having low phase noise.

Thus, we see, the high speed counter problem can be obviated provided a trade-off is accepted.

Because the sideband levels depend upon the scheme used and also upon the output frequency (VCO deviation per uV per-turbation increases with frequency) the treatment of trade-offs is not simple. An attempt has been made, however, to convey a general feel for what to expect. Figure 10 has been prepared to tie together some of the concepts and hardware which have been discussed. Since multiplier input and output frequencies are the basic specified parameters

they appear as axes. The chart shows what kind of scheme would be used for a given input/output frequency combination using no prescaling (top row) and using a  $\div 16$  prescaler (bottom row). To indicate the sideband levels associated with each selection, sideband quality ranges have been indicated as A, B, C, or D, "A" being the best. Sideband levels are related to output frequency, therefore Figure 12 has been included which roughly relates sideband level in dBc (dB below carrier) and multiplier output frequency for each quality range. Neither of these charts should be rigidly interpreted with respect to a specific design as they are intended only to show, quickly, what are the inter-relationships between various goals and to provide a rough quantitative estimate of expected performance.

For example, suppose 100 KHz is to be multiplied up to 50 MHz. Figure 10 shows that if no prescaler is used, a TTL-S pulse swallow counter could be used and the sideband level could be estimated to be level B. Figure 12 shows that at 50 MHz output, level B corresponds to -69 to -82 dBc sideband level. If a prescaler is used, Figure 10 shows that a standard TTL counter can be used but the expected sideband range is -53 to -69 dBc.

A prescale of 16 was chosen for convenience. The prescale can be any easily implemented division ratio preferably a  $2^n$

**Figure 10. Counter Type and Sideband Ranges vs. Input Frequency, Output Frequency, ÷ 16 Prescaler or no Prescaler**

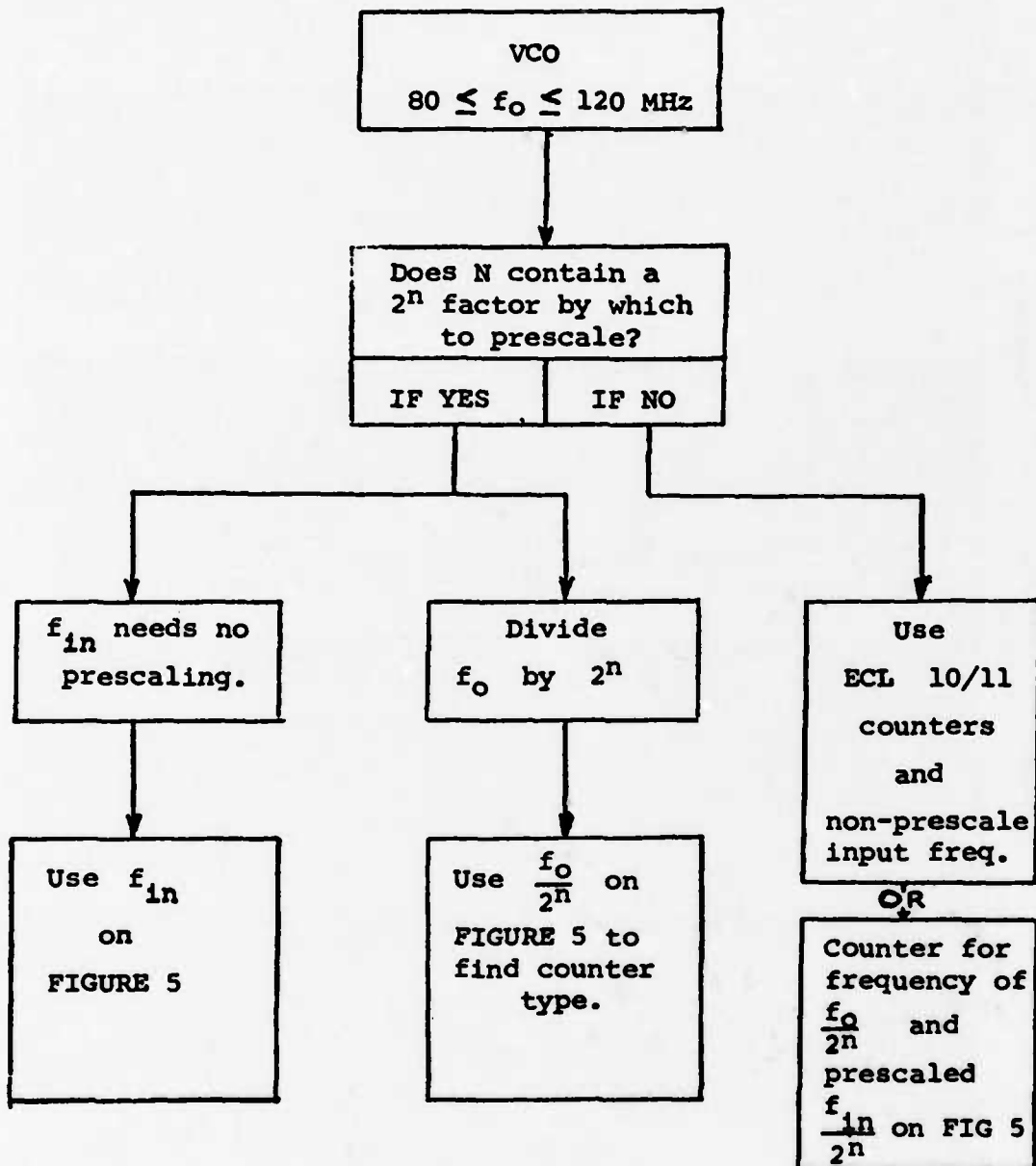


Figure 11. Flow Chart for VCO in the 80 to 120 MHz Range with Options to Prescale by  $2^n$

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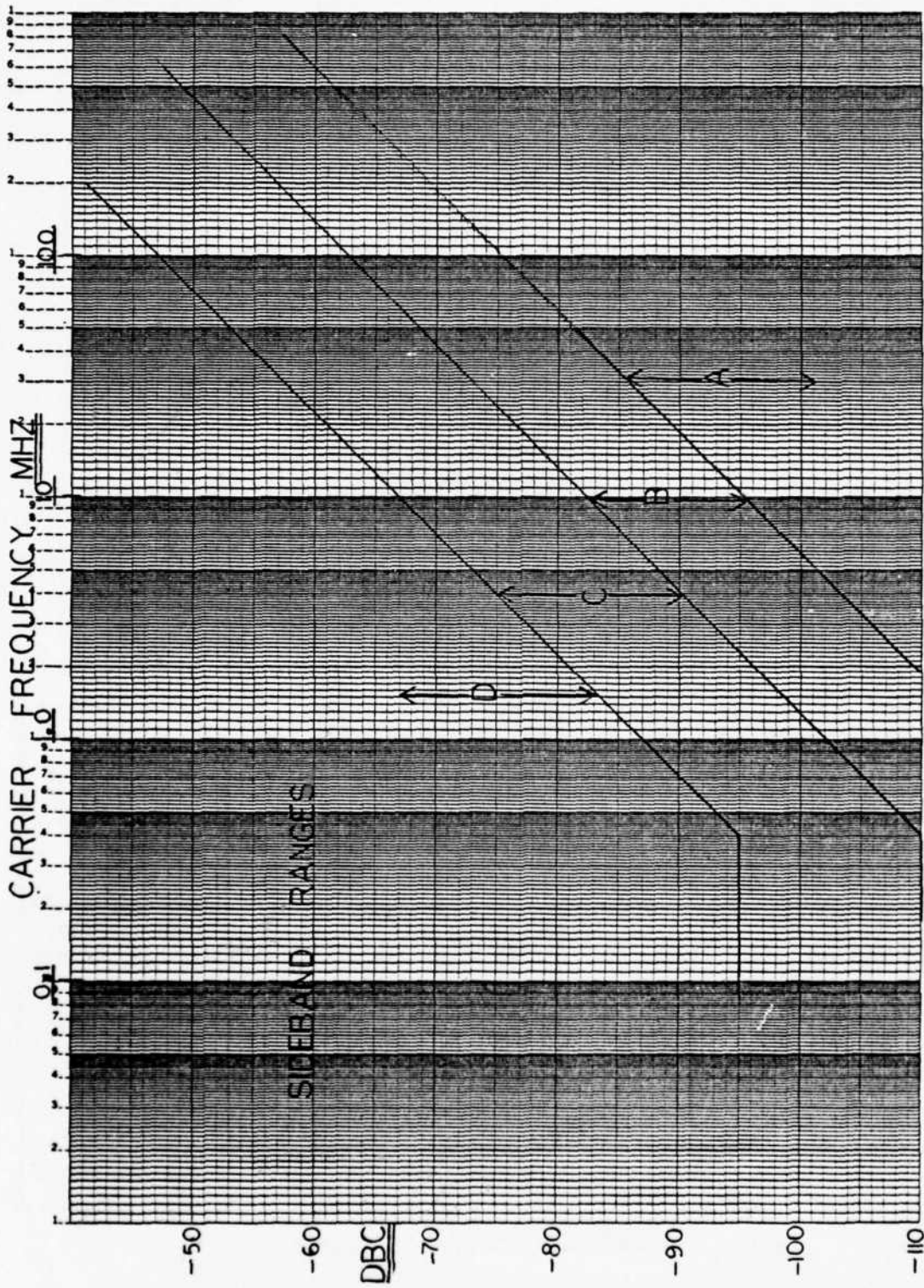


Figure 12. Sideband Ranges

number. Prescaling is particularly important when dealing with output frequencies above 80 MHz which could require ECL counters. A closer look at the options available is presented in Figure 11. A key factor is whether the specified multiplication ratio contains a  $2^n$  factor. If it does, then this factor can be considered a preliminary divider which then drives a lower speed divider which divides by  $N/2^n$ . Thus, the combined dividers comprise an actual divide by  $N$ , above 80 MHz, without the disadvantages of using ECL. If there is no  $2^n$  factor in  $N$  then ECL pulse swallow counters must be used or prescaling of output and input frequencies must be performed. Figure 10 can be used after an option from Figure 11 is selected.

Thus far, an attempt has been made to distill from the general requirement certain cases and certain specific input/output combinations. In this way a rough performance estimate has been presented which is not necessarily the optimum. Only by knowing the particular specifications of a proposed multiplier unit can an optimum scheme be devised.

Also, the hypothetical unit discussed had an implicit level of flexibility, that is, range, of input/output frequencies it could accommodate without redesign. This concept of flexibility has been carried through because the original specification implied a somewhat universal unit having very

large input/output frequency ranges. This kind of unit would be complex and costly and in some ways beyond the capabilities of even the laboratory test synthesizer; for that could not accept input frequencies which are low or which are not specific multiples of 1MHz.

It is felt that a unit which would be most effective would be one which operates between two specified input/output frequencies and with specified phase noise and phase detector sideband levels. The 4MHz phase lock multiplier described later in this report is an example of such a unit.

Within a given system it might be necessary to phase lock two signals whose frequencies are already fixed. In this case, we have no choice of input and output frequencies and the multiplier must be optimized with respect to the available frequencies. The configuration being described now is not intended to have a sizeable degree of frequency flexibility. As a result another degree of control is available; that of using a crystal oscillator instead of an LC oscillator. The basic advantage lies in being able to make the loop bandwidth very small so that adequate filtering of the phase detector frequency is possible. A

crystal controlled phase lock multiplier can work around the difficulties of having a low multiplier input frequency and yet delivering a spectrally clean signal.

Where the choice of input frequency is still open it is important that it be no lower than 100KHz. The output frequency should be less than 80MHz, where possible, to avoid the use of ECL counters.

It has been shown, thus far, that any of the specified input/output frequency combinations can be accommodated quite efficiently through the use of fixed frequency multipliers requiring no unreasonable degree of complexity.

#### SPECIFIC CASE

The unit that was specified for delivery is a phase lock multiplier whose output frequency is 4 MHz at a power level of +12 dBm (15.8 mW) into 50 ohms. The input frequency is 100 KHz  $\pm$  100 Hz or 1000 KHz  $\pm$  1000 Hz. The settling time, measured from the time the input frequency is applied, is specified as  $t_s \leq 10$  ms. The phase noise is to be down 60 dBc at 200 Hz offset and down 100 dBc at 1.2 KHz offset, per Hz bandwidth. Static dividers capable of dividing by 4 and by 40 were to be included.

## 1.2.1

Block Diagram

The multiplier in Figure 13 uses an FET LC oscillator for low phase noise and to permit retuning. The phase detector, at 100 KHz, is a sampled sawtooth (ramp) type whereby the ramp is started by the 100 KHz reference signal and is sampled by the 100 KHz output of the programmable divider. This divider, which is a TTL,  $\div 40$ , divides the 4 MHz VCO signal down to 100 KHz. The loop filter controls the magnitude of the loop bandwidth (1000 Hz) and the phase detector filter attenuates 100 KHz phase detector components which reach the VCO. A phase lock indicator monitors the two 100 KHz phase detector signals.

## 1.2.2

Discussion of Schematic, Circuitry, and Hardware

The VCO is an LC type in a Colpitts configuration. Voltage control is accomplished by means of a varicap CR1. The quiescent voltage on the varicap, when phase locked, is set by adjusting L1 and should not be readjusted. Transistors Q2, Q3, Q4 and Q5 provide isolation and power output capabilities. Transistor Q5 provides the drive to the programmable counter, U1, U2, U3, and U4. Integrated circuits U1 and U2 are counters and U3 and U4 are count recognize gates which generate the pulse which resets U1 and U2. These are binary counters and thus have a maximum of sixteen counts each. The four IC's are presently programmed to count to 40. The 100 KHz output pulse appears at pin 8 of U3.

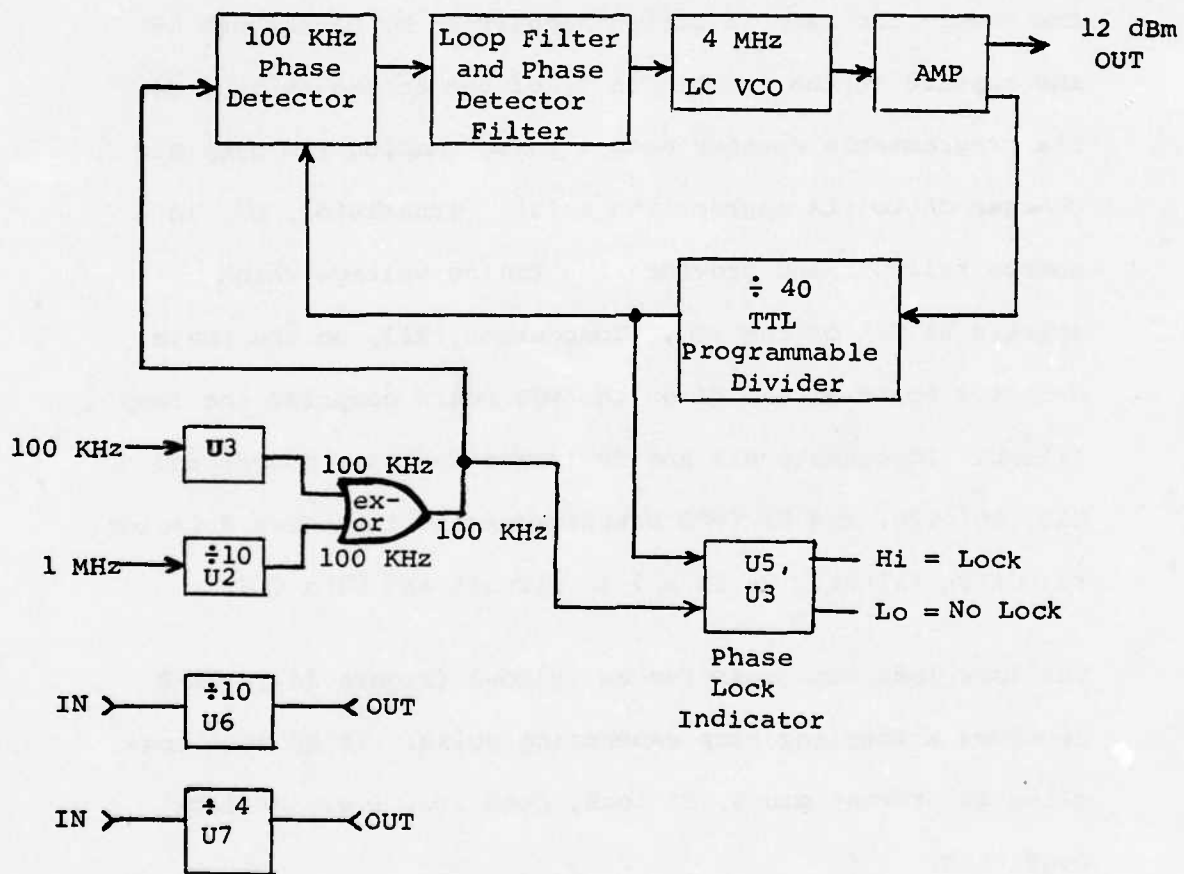


Figure 13. 4 MHz Phase Lock Multiplier, Block Diagram

The phase detector is the sampled sawtooth type. Current from Q2 charges capacitor C5 in a linear voltage ramp of about 9 volts maximum. A .100 KHz input frequency pulse into Q1 causes Q1 to short C5 to ground thereby resetting the ramp. The ramp is current amplified by Q3 through Q6 and appears at the input, pin 9, of the analog switch, U4. The programmable counter output pulse samples the ramp and charges C6 to its appropriate value. Transistor, Q7, is a source follower and provides the tuning voltage which appears at CR1 of the VCO. Components, R13, on the phase detector board R1 and C1 on the VCO board comprise the loop filter. Components R13 and C8 (phase detector board) and C19, L8, C20, and R1 (VCO board) comprise the phase detector rejection filter. U6 is a  $\div 10$  circuit and U7 a  $\div 4$ .

The lock indicator operates as follows (Figure 14). U5-9 receives a toggling ramp generating pulse. If no such toggling is present pin 5, HI lock, goes low, i.e., no lock condition.

U5-10 & 11 need "highs" from U5-13 which occurs when the counters sample pulse is toggling at U5-1 and when U5-3 is simultaneously high.

U5-3 is high only if U3-4 is low (sinking current). U3-4 cannot be low if U3-2 is receiving a high (i.e., the ramp is resetting to zero volts) and U3-1 is receiving a low (i.e.,

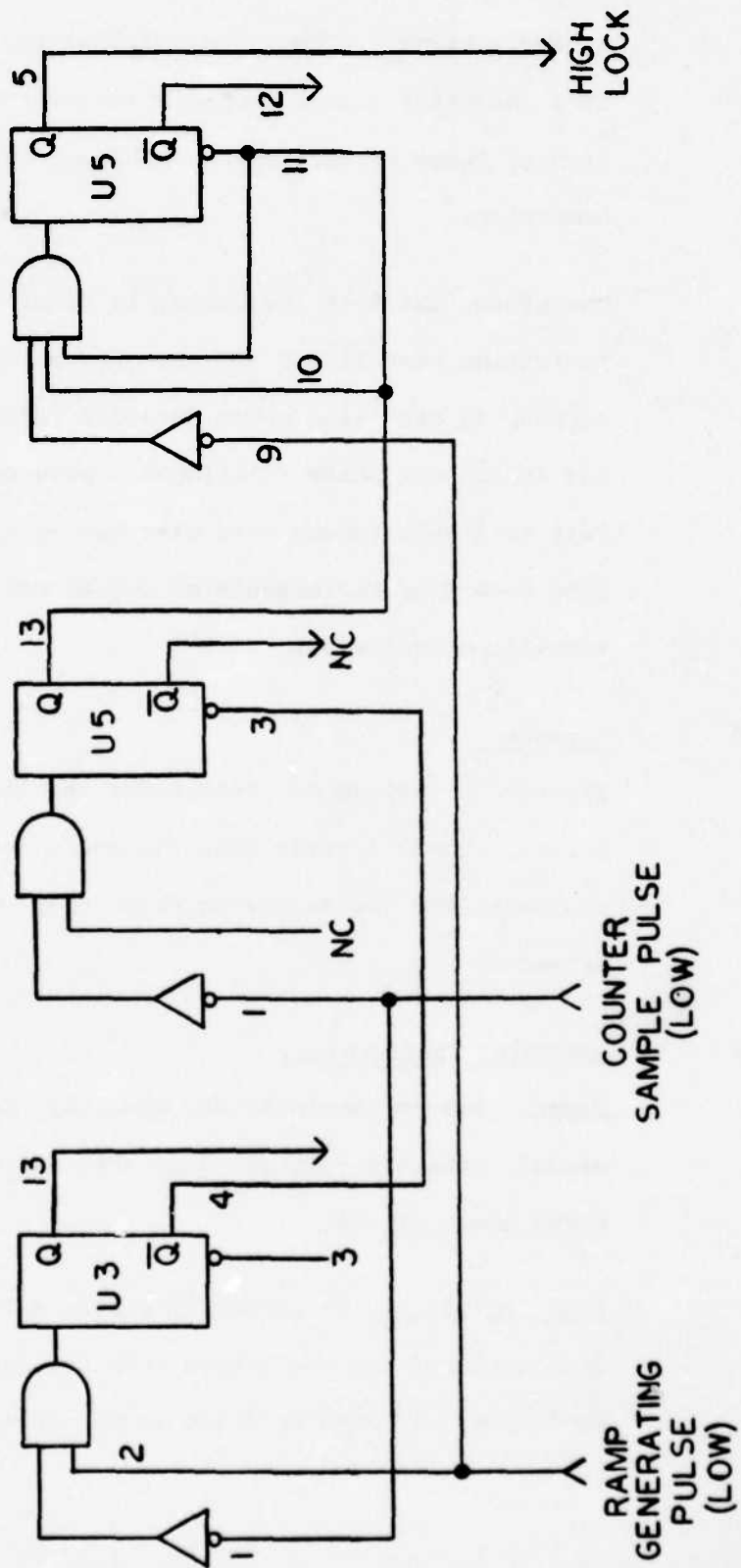


Figure 14. Lock Indicator Circuit

a sample pulse). Thus, U3-4 will go low and inhibit U5-3 if a (negative going) sample pulse over arrives when the ramp is being reset, which can happen only in an out-of-lock condition.

Therefore, the lock indicator, in order to present a lock indication must have 5 VDC present, an operating counter output, an operating phase detector reference (ramp) input, and an in-lock phase relationship between these two signals. This fail-safe scheme precludes having a false lock indication caused by the absence of one or more of the necessary signals, or voltages.

#### 1.2.3

##### Results

Figures 15 through 18 present the results of the design effort. These figures show the goals set forth in the work statement and the degree to which they were met and/or exceeded.

#### 1.2.4

##### Operating Instructions

Power: Solder terminals are available for all voltages and ground. The  $\pm 12$  voltages draw about 45 mA and the +5 voltage draws about 220 mA.

Lock Indicator: As presently wired, a TTL high between the lock terminal and the ground terminal indicates an in-lock condition. If used to light an LED directly, no more than

<u>CHARACTERISTIC</u>	<u>GOALS</u>	<u>PERFORMANCE</u>
Input Frequency	100 KHz $\pm$ 100 Hz 1000 KHz $\pm$ 1000 Hz	+ 1 KHz 100 KHz - 2 KHz  +10 KHz 1000 KHz -20 KHz
Settling Time	Less Than 10 ms	$t_s = 1$ ms
Phase Spectral Density	At 200 Hz Offset, -60 dBc/Hz At 1200 Hz Offset, -100 dBc/Hz	-90 dBc/Hz -115 dBc/Hz
Output Level	+12 dBm (15.8 mW)	19 mW
Fixed Divider	Divider To Be Capable Of $\div 4$ and also $\div 40$	Divider capable of $\div 4$ , $\div 10$ , and $\div 40$
Output Harmonics	Not Specified	2nd, -28 dBc; 3rd, -33 dBc; 4th, -48 dBc
100 KHz Reference Sideband Levels	Not Specified	100 KHz, -105 dBc; 200 KHz, -98 dBc
DC Input Power	Not Specified	+12V, 45 mA; -12V, 45 mA; +5V, 220 mA
Phase Lock Indicator	Not Specified	Indicates that both phase detector inputs are present and that they are phase locked.

Figure 15. AFAL Modem Building Blocks,  
Phase Lock Multiplier SN 1

<u>CHARACTERISTIC</u>	<u>GOALS</u>	<u>PERFORMANCE</u>
Input Frequency	100 KHz $\pm$ 100 Hz	100 KHz + 1.4 KHz - 1.5 KHz
	1000 KHz $\pm$ 1000 Hz	1000 KHz + 14 KHz - 15 KHz
Settling Time	Less Than 10 ms	$t_s = 1$ ms
Phase Spectral Density	At 200 Hz Offset, -60 dBc/Hz	-87 dBc/Hz
	At 1200 Hz Offset, -100 dBc/Hz	-115 dBc/Hz
Output Level	+12 dBm (15.8 mW)	+15 dBm
Fixed Divider	Divider to be capable of $\div 4$ and also $\div 40$	Divider capable of $\div 4$ , $\div 10$ , and $\div 40$
Output Harmonics	Not Specified	2nd, -29 dBc; 3rd, -31 dBc; 4th, -49 dBc
100 KHz Reference Sideband Levels	Not Specified	100 KHz, -103 dBc; 200 KHz, -98 dBc
DC Input Power	Not Specified	+12V, 45mA; -12V, 45 mA; +5V, 220 mA
Phase Lock Indicator	Not Specified	Indicates that both phase detector inputs are present and that they are phase locked.

Figure 16. AFAL Modem Building Blocks,  
Phase Lock Multiplier SN2

<u>CHARACTERISTIC</u>	<u>GOALS</u>	<u>PERFORMANCE</u>
Temperature Range	Normal Room Temp.	Over $0^{\circ} \leq T \leq 75^{\circ}\text{C}$ Temp. Sensitivity is insignificant.
Input Drive	Not Specified	TTL or 1V rms sine wave.
Input Duty Cycle	Not Specified	Not Duty Cycle Sensitive.

Figure 17. SN1 and 2

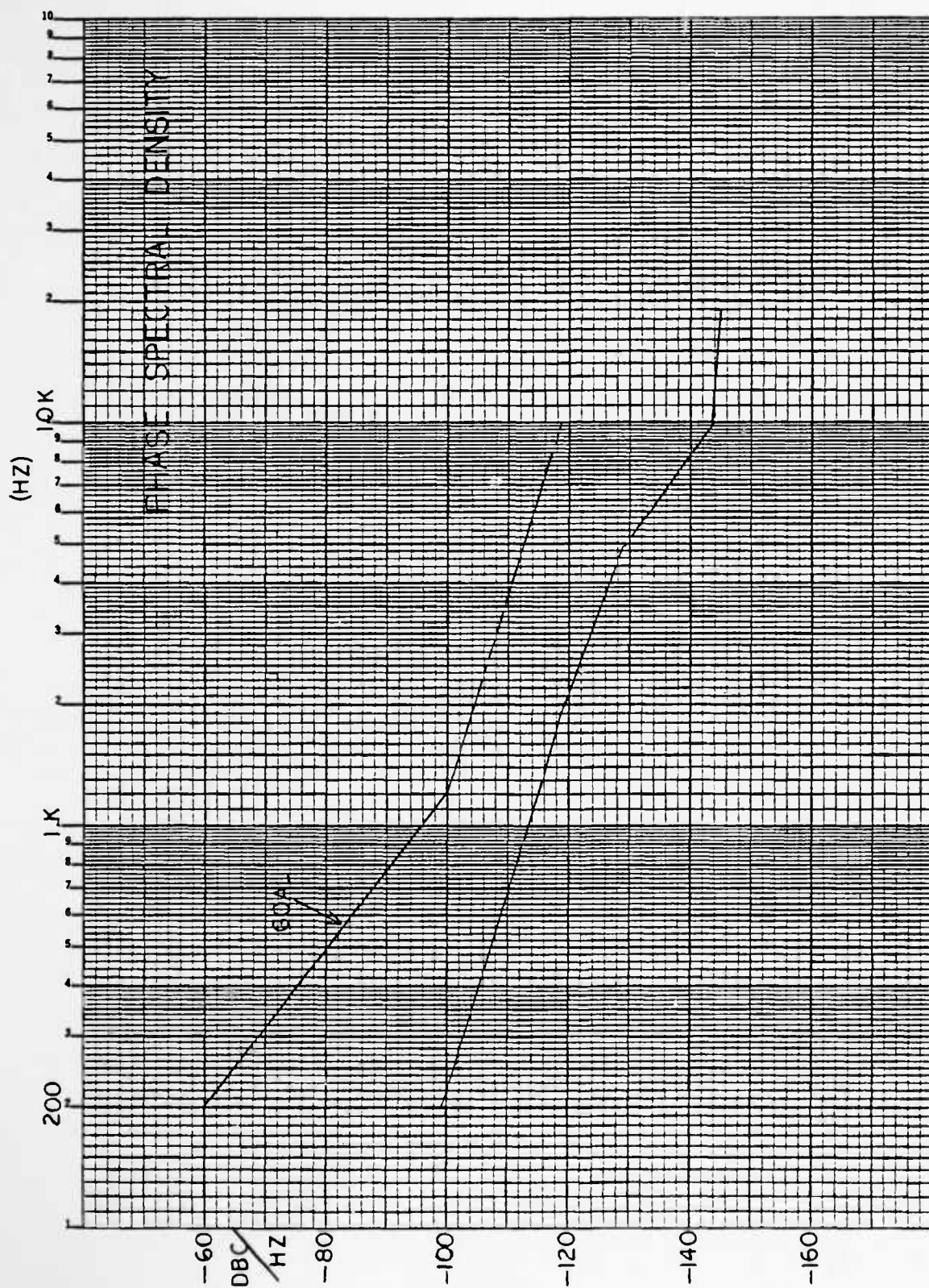


Figure 18. Phase Spectral Density

3 mA should be drawn. A resistor should be placed in series with the LED to accomplish this. To drive an incandescent indicator, drawing perhaps 40 mA, an external lamp driver circuit must be used. (Note that a terminal has been provided for U5-12 so a low logic level may be used as an indication of lock if necessary.)

Input connections: The input to the unit consists of the application of 1 MHz to the 1 MHz IN jack or 0.1 MHz to the .1 MHz IN jack. As the input selection is performed automatically only one input should be applied at any one time. The input signal may come from the driver with a TTL totem pole output or with a sinewave a.c. coupled output. If the latter, the sinewave must be at least one volt rms. The input connector is BNC.

Output connections: The output connector is BNC and will deliver a 12 dBm (minimum) sinewave into a 50 ohm resistive load. Non-resistive or non-linear loads which are not adequately isolated will, of course, distort the output waveform.

Fixed dividers: The fixed  $\div 4$  and  $\div 10$  dividers can be driven by a TTL totem pole driver or a 1V rms sinewave. Their outputs are TTL totem pole outputs. Either of the inputs can be driven by the 4 MHz output connector which is also driving a 50 ohm resistive load. If an isolation

amplifier is used no degradation of any of the multiplier's output specifications results. If no isolation amplifier is used then, of course, some of the divider's output frequency also appears at the multiplier output jack at more than 50 dB below the 4 MHz signal. To effect division by 40 a jumper of coaxial cable should connect the  $\div 4$  output to the  $\div 10$  input.

Cover removal: To remove cover marked 6656 simply remove the eleven screws on the cover. The other cover, marked 6655, removes by removing only the two unpoxied screws and by removing the opposite 6656 cover.

## 1.2.5

Reprogramming and Modification Instructions(a) VCO

The amplifiers following the VCO were deliberately made broadband so that the VCO frequency could be changed if desired. This most properly should be considered an engineering design function and should be done by personnel who are knowledgeable in the areas of RF circuit and phase lock loop design. In general, however, to change the VCO frequency the reactances, represented by L1, C4, C5, and CR1, should be maintained at the new frequency. Even then, some optimization might be needed. In this unit the highest frequency the VCO should be adjusted to is 10 MHz due to the limitations of the programmable counter it drives.

(b) Module N Counters

The programmable counter can be reprogrammed to count from 2 to 255. Figure 19 shows a photographic detail of the VCO/counter PCB. Shown are counters U1 and U2 along with their respective programming terminal posts. Within each terminal post array are two posts labeled "0", and are logic zeroes, in this case ground. Two more posts are labeled "1" and are logic ones, in this case 4 VDC. Included also are posts labeled A, B, C, D where A is the  $2^0$  bit, B the  $2^1$  bit, C the  $2^2$  bit, and D the  $2^3$  bit of the preset load to the counter IC. When U4, the end of count recognize gate, generates a reset pulse the binary coded decimal (BCD) number on lines A, B, C, and D is loaded into the counter thus presetting it to that count before the count sequence begins. Each counter, U1 and U2, has an ABCD array on the board. Modulo 16 up counters have been used which start at zero and count to 15. Therefore, to get the counter to count twice before resetting to zero one must preset it to 13; that is, the 15's complement of 2. The accompanying chart, Figure 20, contains all the division ratios up to 255 and indicates the programs of U1 and U2 which will enable the counter to perform the necessary count. Data lines, A, B, C, and D are to be hand wired to the nearest logic "0" or "1" terminal posts on the PCB.

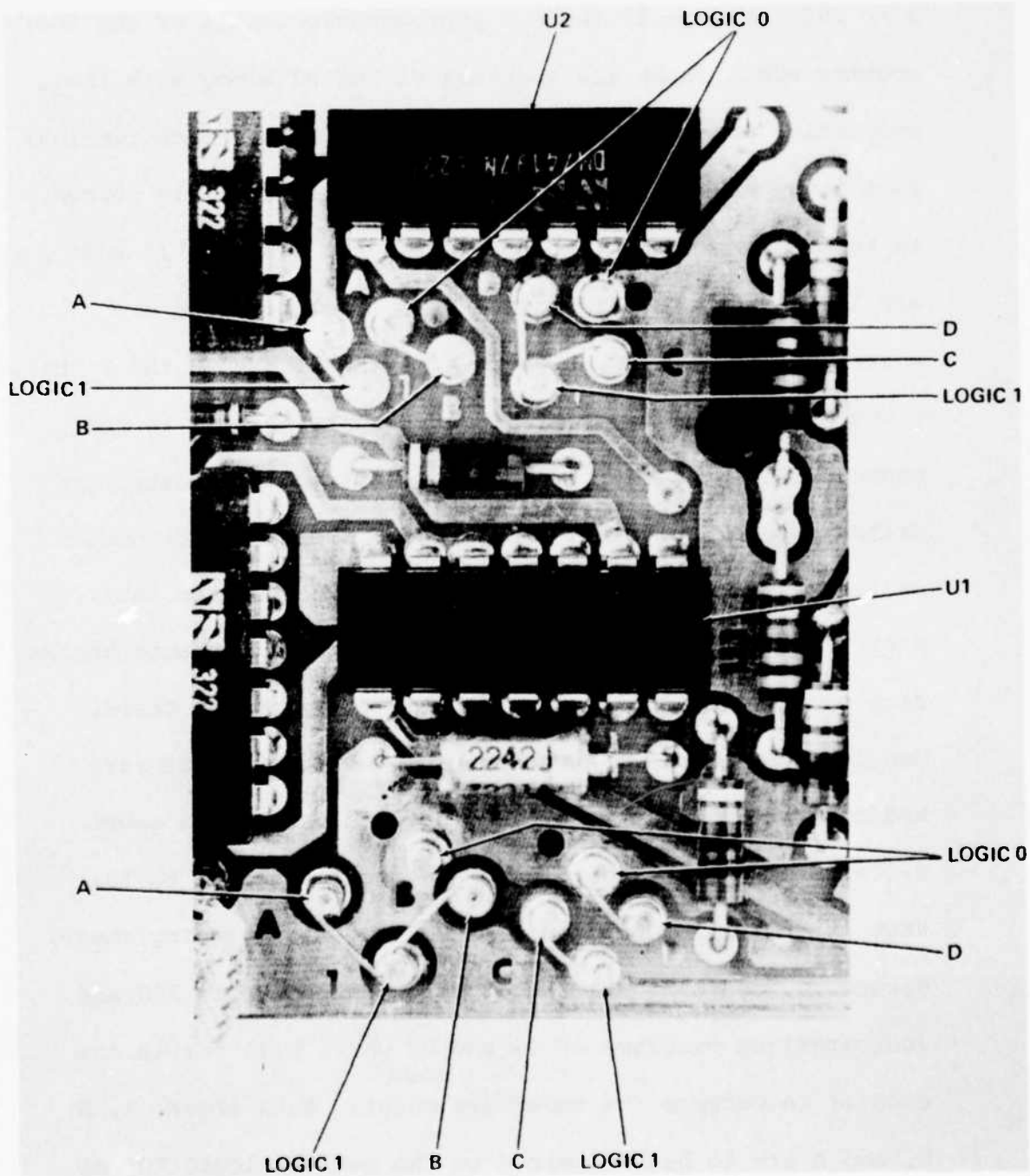


Figure 19. VCO/Counter PCB

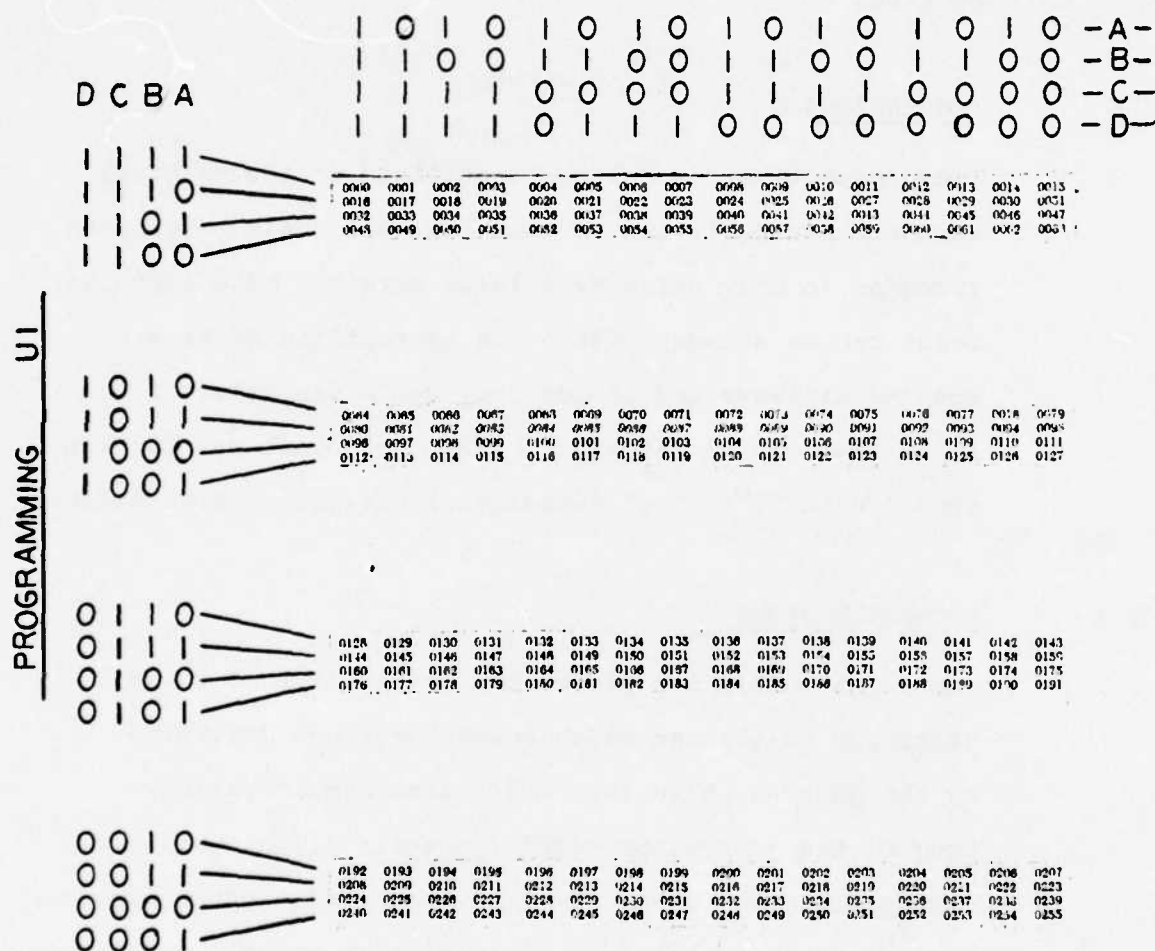


Figure 20. Programming U2

(c) Lock Indicator

If a logic low is needed to provide an external lock indication then the terminal connected to U5-12 may be used.

1.3

CONCLUSIONS

From inspection of the goals outlined on the original work statement, it can be seen that all goals have been exceeded in many cases by a large margin. Note that the input can be standard TTL or an appropriate level a.c. coupled sinewave and is not duty cycle sensitive, a point that was of concern to AFAL. The unit was checked from 0°C to 75°C. All temperature effects were negligible.

1.4

RECOMMENDATIONS

The 4 MHz multiplier proves the feasibility of fixed frequency multiplier which cover the range described by the general phase lock multiplier specification. Many of the general multiplier specifications were realized in this unit. To implement a more generalized, more flexible multiplier, would require greater complexity.

<u>SELECTABLE PARAMETER</u>	<u>RECOMMENDATION</u>
OUTPUT FREQUENCY	SHOULD BE LESS THAN 80MHz
INPUT FREQUENCY	SHOULD BE GREATER THAN 100KHz
RATIO OF OUTPUT TO INPUT FREQUENCY	RATIO SHOULD CONTAIN AS MANY FACTORS OF 2 AS POSSIBLE

Figure 21. Guide to Frequency Multiplier Specs

In specifying frequency multipliers of this nature it is essential to make the best choice of input and output frequencies. An output frequency which is unnecessarily high could require the frequency counters to use emitter coupled logic (ECL), which is not a convenient logic family to use.

Thus, the output frequency selected should be below 80 MHz and lower still, where possible.

The input frequency should be as high as possible to provide good spectral purity as it is difficult to prevent a low input frequency from appearing on the output frequency signal. Input frequencies above 100 KHz fall into an acceptable range. Lower input frequencies are particularly troublesome because they produce sidebands in the very area where low phase noise is typically specified.

In selecting an input/output frequency combination it would greatly simplify matters if these frequencies were related by as large a  $2^n$  factor as possible, i.e.,  $f_o = 2^n f_{in}$ . This would permit prescaling  $f_o$  with divide-by-two flip-flops before further division by low speed variable modulus counters, which then divide by  $N/2^n$ .

If a  $2^n$  factor is not present in the multiplication ratio then, at frequencies exceeding 80 MHz, either ECL counters must be used or both, the output and input frequencies must

be scaled down by a common prescaling factor. The latter technique can degrade spectral purity because the phase detector would be operating at a lower frequency. The trade-offs would have to be weighed. Figures 10, 11 and 12 can be used to obtain a rough quantitative estimate of trade-offs, schemes, critical frequencies and counting moduli.

If a phase detector frequency less than 100KHz must be used (because of prescaling or low input frequency) and very good spectral purity (SB-A levels), in the form of low sideband levels, is specified, then a crystal oscillator could be used within a very small phase lock loop bandwidth. In this case, the flexibility of being able to generate a different output frequency, by reprogramming the counters, is lost but a very clean output signal is gained.

Where it is essential to minimize size and weight, the possibility of LSI packaging should be considered. For necessary isolation, separate circuits such as the VCO, programmable counters, phase detector and lock circuits, could be placed on separate LSI substrates thus contributing to a large size and weight reduction.

Where a very flexible frequency multiplier is desired, one that would accept several widely separated input frequencies

and output frequencies, a large increase in size, weight, complexity, and cost must be expected. What determines complexity is the amount of additional circuitry needed to accommodate the desired flexibility. This depends upon the specific input and output frequencies selected. If the frequency ranges are small or if the frequencies within the range are integrally or rationally related then it is possible to maintain a simple, but modified, scheme. On the other hand, widely divergent or unrelated input frequencies or output frequencies usually prevent a high degree of circuit commonality.

It is hoped that this section has given some insight into the techniques of building a phase lock frequency multiplier and that it may aid AFAL in specifying frequency multipliers which might fill any of its prospective needs.

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SECTION II

AFAL COSTAS DEMODULATOR STUDY

2.1. GENERAL CASE

2.1.1 PSK Modulation

2.1.1.1 Definition

Phase Shift Keying is a form of angle modulation in which the phase angle of a continuous frequency carrier assumes one value chosen from a finite set of discrete values representing all allowed information symbols.

2.1.1.2 Description

PSK modulation is usually restricted to M discrete phases representing N bits of information per symbol, thus relating N and M by the following equation.

$$2^N = M \qquad \text{EQ. 1}$$

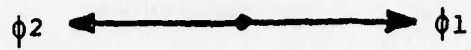
From this relation one may see that with N increasing linearly (1, 2, 3, 4, etc.) M increases exponentially (2, 4, 8, 16, etc.) and thus the finite set of M discrete phases or symbols becomes unwieldy very rapidly, as shown in Figure 22. For this reason one typically limits N to some small number, the most common being one or two.

Communication through a noisy medium is shown in Figure 23 and this also helps to explain why N is kept small. The angle estimator or demodulator must provide a best estimate of the carrier phase during a symbol period, but the carrier now has random angle modulation due to the noise added to the carrier during its transmission over the

$$N = 1 \quad M = 2$$

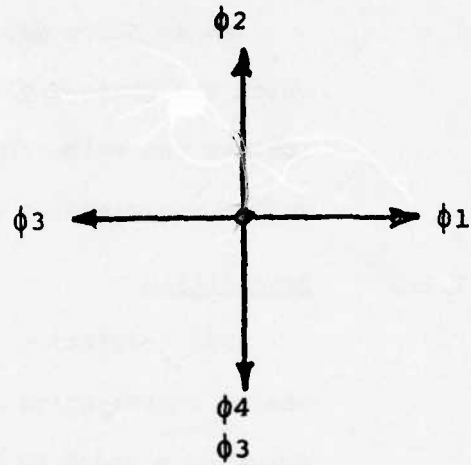
$$M_1 \leftrightarrow \phi_1$$

$$M_2 \leftrightarrow \phi_2$$



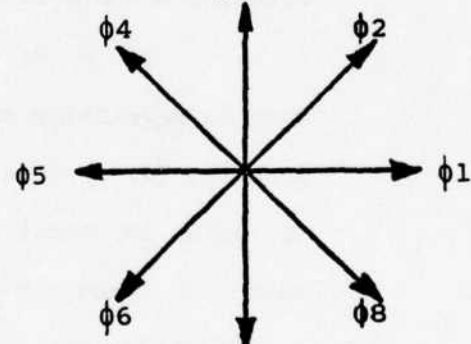
$$N = 2 \quad M = 4$$

$$M_1 \leftrightarrow \phi_1$$



$$N = 3 \quad M = 8$$

$$M_i \leftrightarrow \phi_i$$



$$N = 4 \quad M = 16$$

$$M_i \leftrightarrow \phi_i$$

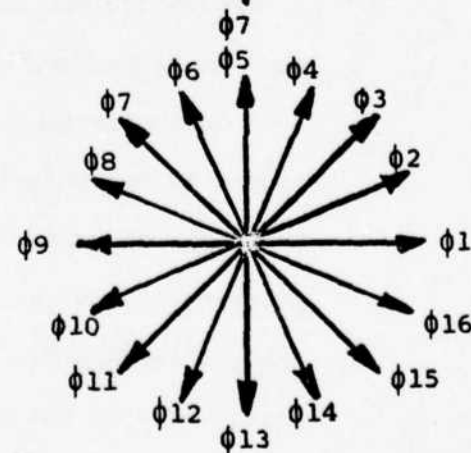


FIGURE 22. Increase of M Versus N

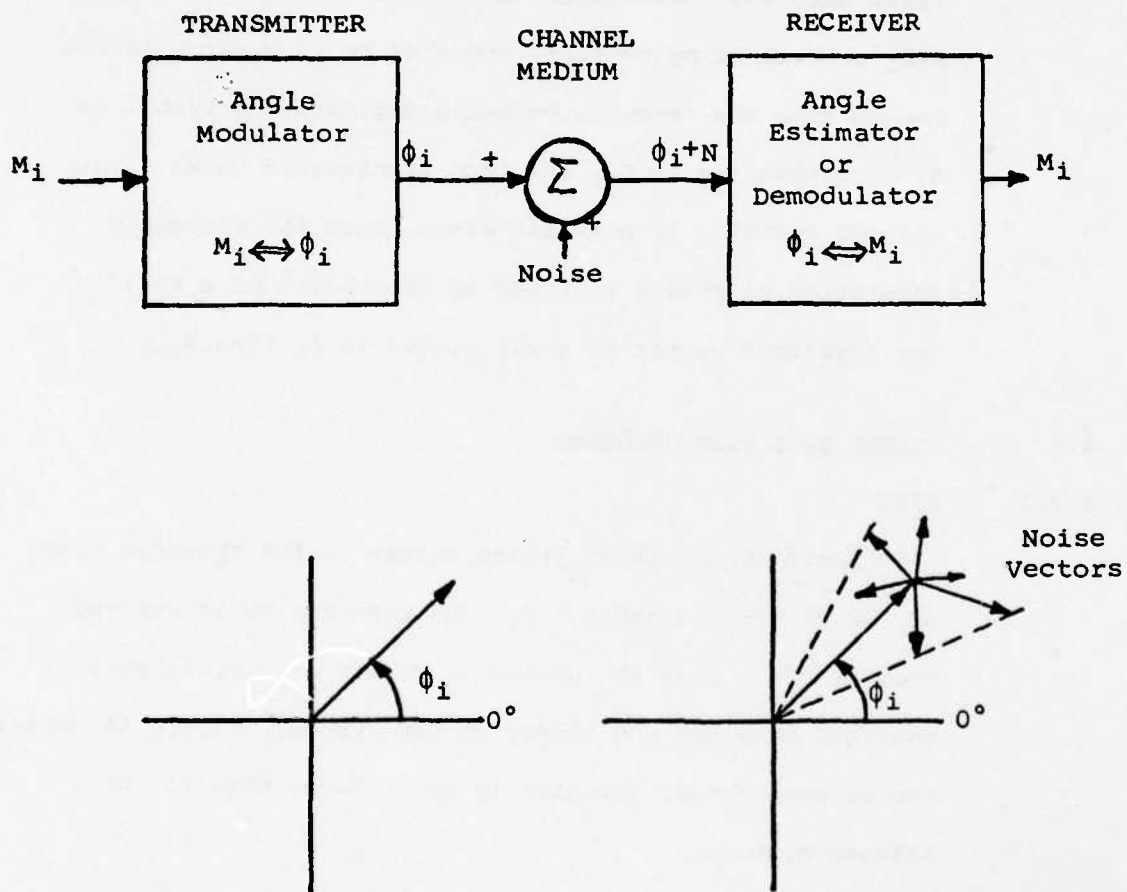


Figure 23. PSK Communications Link

channel medium.

Figure 24 compares the cases of large  $N$  versus small  $N$ . In both instances, phase  $\phi_1$  was sent and the same noise vector was assumed to be added to the signal vector, with the resultant vector shown as a dashed line. In the first case the demodulator would estimate the symbol as  $M_{i+1}$  corresponding to  $\phi_{i+1}$ , and thus be in error. In the second case the demodulator would estimate the symbol as  $M_1$  corresponding to  $\phi_1$ , the true transmitted phase. This correct decision is possible since, with the increased separation of phases provided by the choice of a small  $N$ , the resultant vector is still closer to  $\phi_1$  than  $\phi_{i+1}$ .

## 2.1.2 Common Modulation Schemes

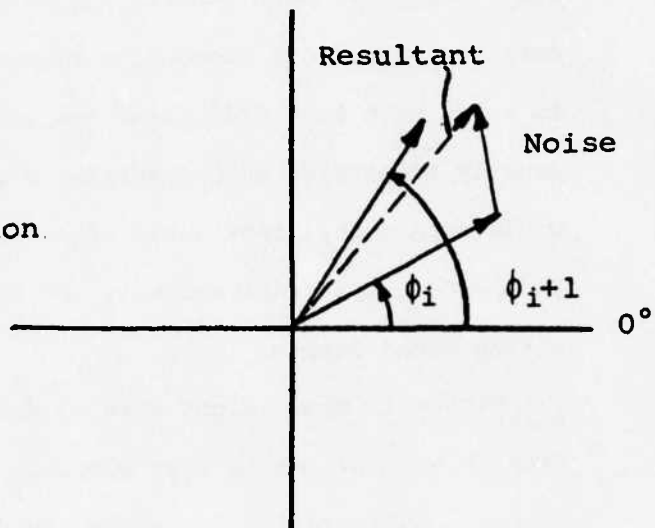
### 2.1.2.1 BPSK

Binary Phase Shift Keying refers to the specific case of PSK with  $N = 1$  and  $M = 2$ . The term Binary is derived from the fact that the number of phases or symbols used is two, the base for the binary number system. Figure 25 depicts the allowed phases graphically and relates them to the allowed symbols.

### 2.1.2.2 QPSK

Quadri-Phase Shift Keying describes the specific case of PSK with  $N = 2$  and  $M = 4$ . The prefix Quadri- arises from the use of four phases. The basic characteristics of QPSK

Large N  
Small Separation  
of  $\phi_i + \phi_{i+1}$



Small N  
Large Separation  
of  $\phi_i + \phi_{i+1}$

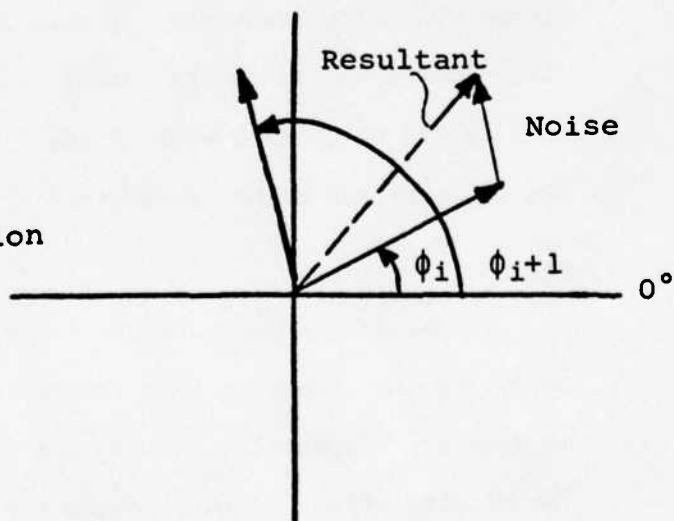


Figure 24. Effects of Noise on Selection of N

are shown in Figure 26. By comparing the phasor diagram for BPSK in Figure 25 and QPSK in Figure 26, one notices that QPSK consists of two BPSK signals positioned orthogonally with respect to each other. The two phasors  $\phi_0$  and  $\phi_0 + 180^\circ$  form one signal set commonly designated I channel, and  $\phi_0 + 90^\circ$  with  $\phi_0 + 270^\circ$  forms the second signal set which is usually identified as Q channel. From this observation, one would expect that QPSK could be generated and detected as two independent BPSK data streams, and this turns out to be true within broad limits.

Figure 27 shows eight bits of data encoded two bits at a time ( $N = 2$ ) as one of four possible phases ( $M = 4$ ). Two methods of generation are shown, the first is direct QPSK encoding and the second is generation via summation of two independent BPSK signals. Note that the resultant transmitted phasor is identical for both methods of composition. Also significant is the fact that the transmitted RF symbol rate is one half ( $\frac{1}{N}$ ;  $N = 2$ ) of the digital data rate since two ( $N$ ) bits are being transmitted every symbol.

#### 2.1.2.3 SQPSK

Staggered Quadri-Phase Shift Keying is identical to QPSK with the exception that the orthogonal I and Q BPSK signals are staggered or offset one digital data bit in time. The primary effect of this staggering is to eliminate simultaneous changes in both the I and the Q channels.

$$\begin{array}{ccc}
 & N = 1 & M = 2 \\
 \left. \begin{array}{l} M_1 = \phi_0 \\ M_2 = \phi_0 + 180^\circ \end{array} \right\} & \text{Possible Assignment \#1} & \\
 \left. \begin{array}{l} M_1 = \phi_0 + 180^\circ \\ M_2 = \phi_0 \end{array} \right\} & \text{Possible Assignment \#2} &
 \end{array}$$

$\phi_0 + 180^\circ$   $\longleftrightarrow$   $\phi_0$  Phasor Diagram

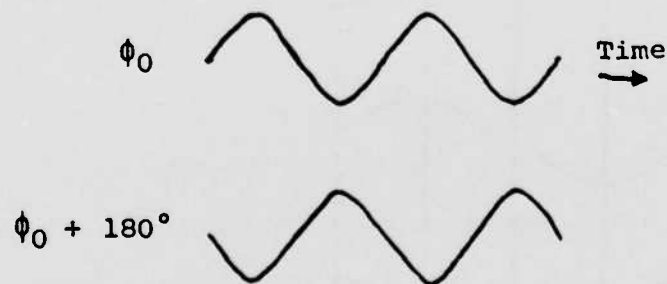


Figure 25. BPSK

$$N = 2$$

$$M = 4$$

$$M_1 = \phi_0$$

$$M_2 = \phi_0 + 90^\circ$$

$$M_3 = \phi_0 + 180^\circ$$

$$M_4 = \phi_0 + 270^\circ$$

One Assignment of  
24 possible.

$$M! = 24; M = 4$$

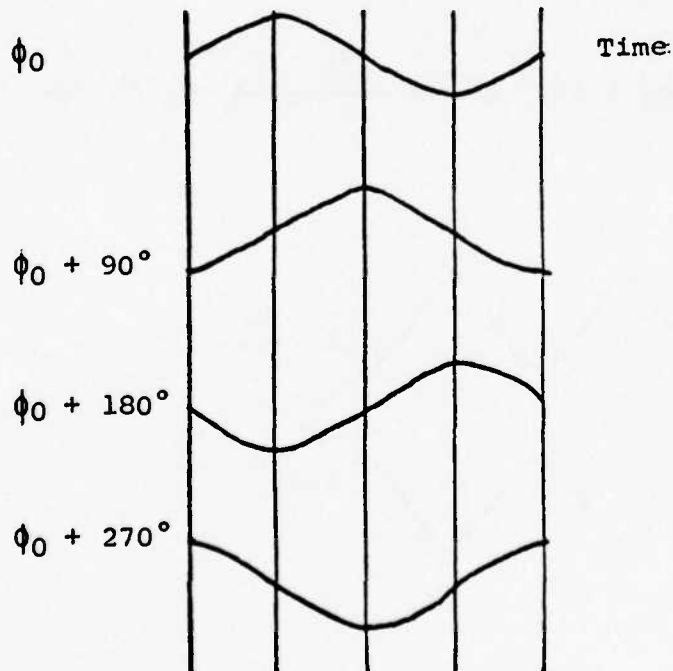
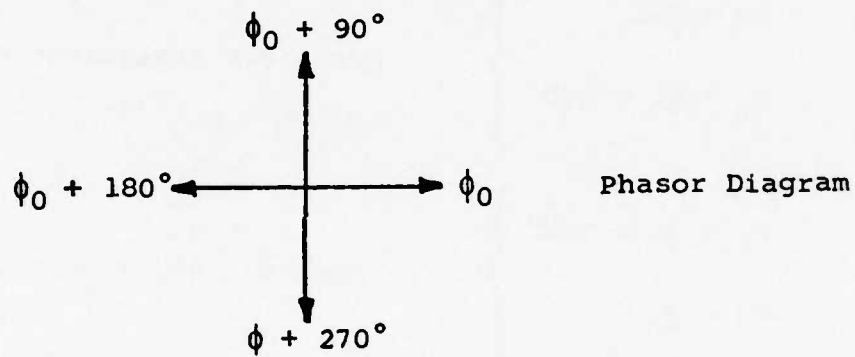


Figure 26. QPSK

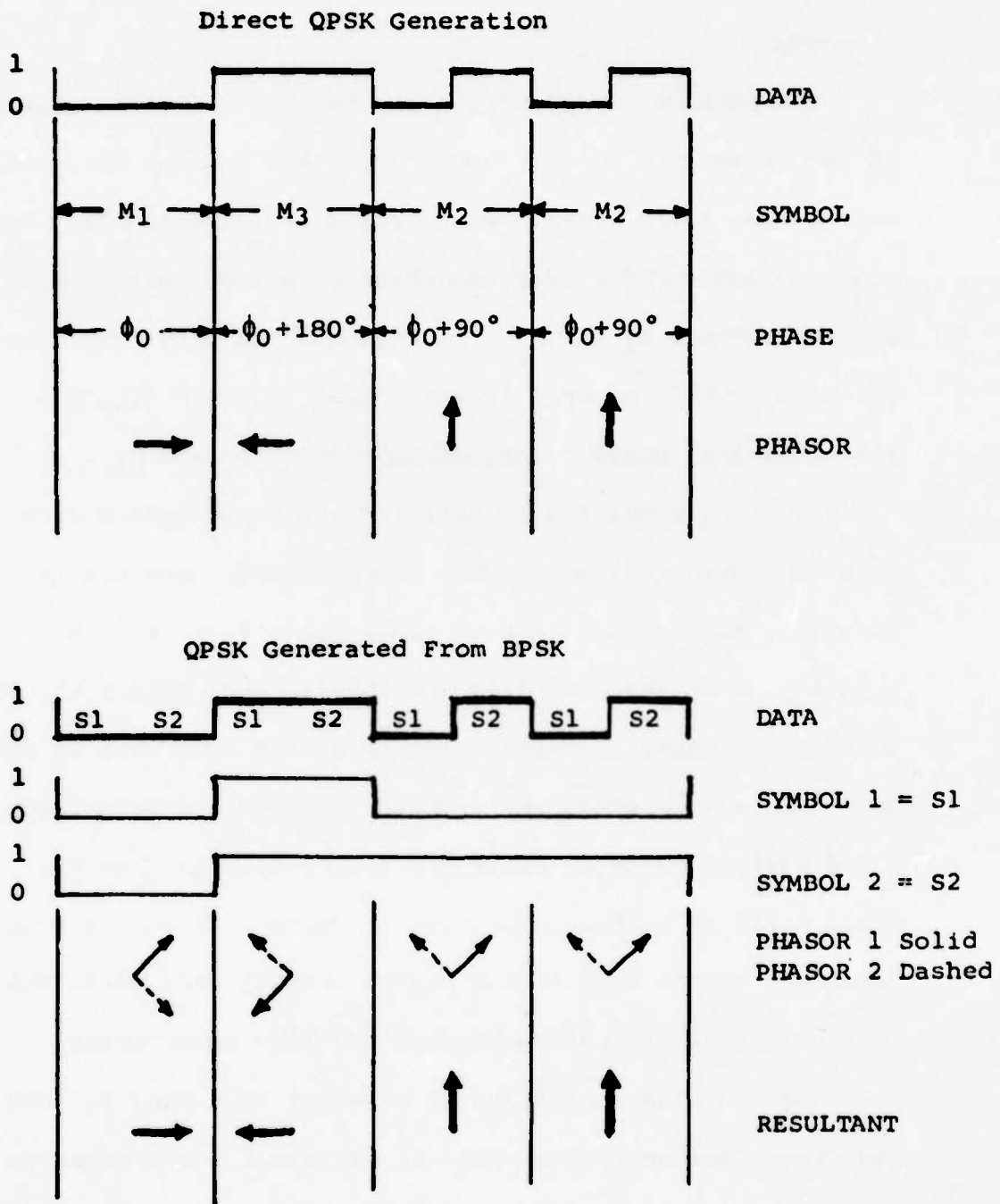


Figure 28 shows the timing necessary to generate SQPSK by splitting a data stream into two staggered orthogonal channels.

The purpose of staggering the two I and Q BPSK signals is the prevention of very large amplitude modulation in the output when a  $180^\circ$  phase shift occurs instantaneously. Referring to Figure 27 for QPSK one observes a  $180^\circ$  phase change between symbols  $M_1$  and  $M_3$ . In Figure 26 the phase assignment for each symbol, as well as the phasor and time diagrams show this  $180^\circ$  phase relationship between  $M_1$  and  $M_3$ .

Figure 29 shows the RF output signal amplitude versus time for both QPSK and SQPSK. In QPSK as  $\phi_0$  dies out or decays at the natural rate of the system,  $\phi_0 + 180^\circ$  is building up at the same rate and this is what causes the RF envelope to decay to zero amplitude at the time when  $\phi_0$  and  $\phi_0 + 180^\circ$  are of equal amplitude. The vector diagrams show the different paths by which the signal changes from one phase state to another, and from these one can see that the amplitude of the QPSK signal passes through zero while the SQPSK signal never passes through the zero power point.

The usefulness of SQPSK is greatest in a band limited, amplitude limited system where an AM signal would generate higher postlimiting sidebands than a signal without AM modulation.

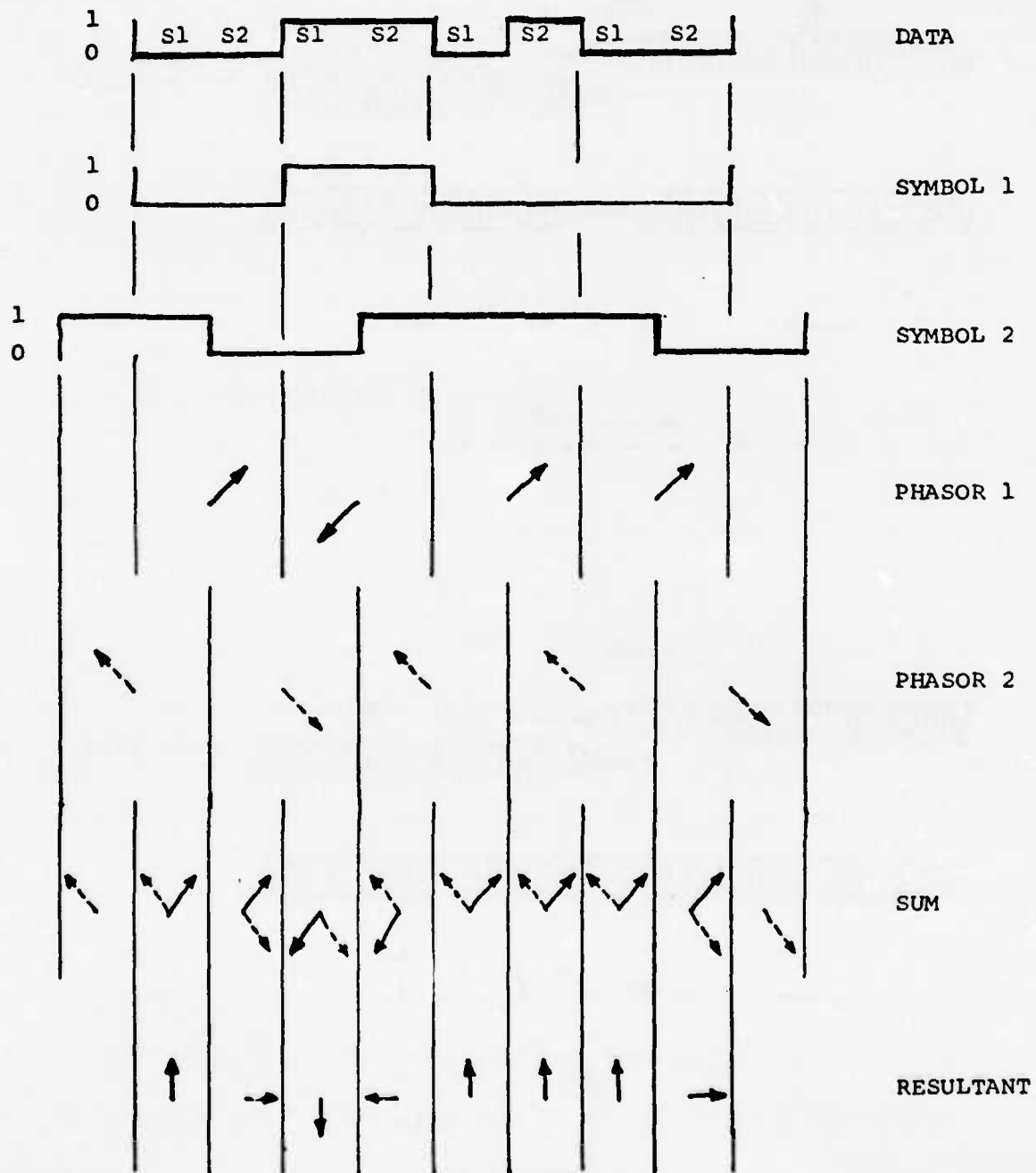


Figure 28. SQPSK Generation

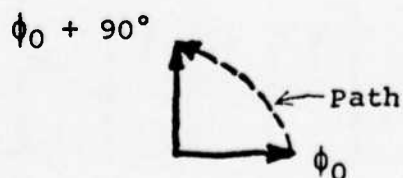
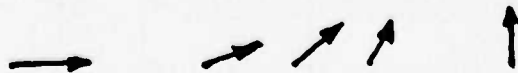
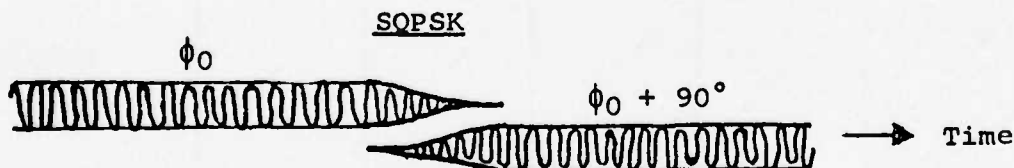
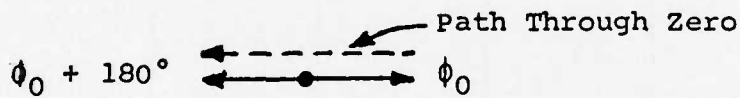
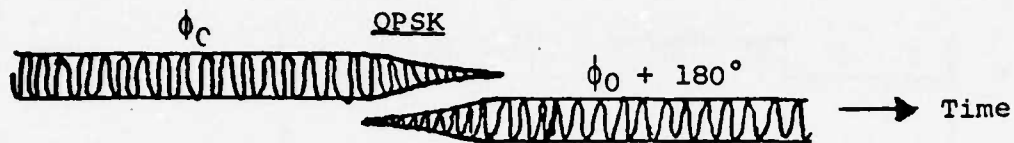


Figure 29. QPSK Vs. SQPSK, Rf Output Signal Amplitude vs. Time

#### 2.1.2.4 Comparison of BPSK, QPSK, & SQPSK

In order to examine the aforementioned methods of modulation one must assume some constant quantity as a basis for comparison. Since the purpose of all three forms of PSK is to transfer information, we will assume a constant digital data rate of  $R$  bits per second. We will further assume that the digital data is completely random with the probability of a one equal to the probability of a zero.

It can be shown that the frequency spectrum of a series of constant amplitude, constant width ( $T = 1/R$ ), random polarity pulses is defined by the following equation.

$$F(f) = \frac{\sin\left(\frac{\pi f}{R}\right)}{\left(\frac{\pi f}{R}\right)} \quad \text{EQ. 2}$$

If we square the above, the power spectral density is readily obtained.

$$G(f) = \frac{\sin^2\left(\frac{\pi f}{R}\right)}{\left(\frac{\pi f}{R}\right)^2} \quad \text{EQ. 3}$$

Figure 30 shows both the frequency spectrum as well as the power spectral density.

The power spectral density as shown in Figure 30 is the most common representation of the random data sequence in the frequency domain since most equipment used to display this domain does not have a phase information display, but shows only the power present at discrete frequencies. One

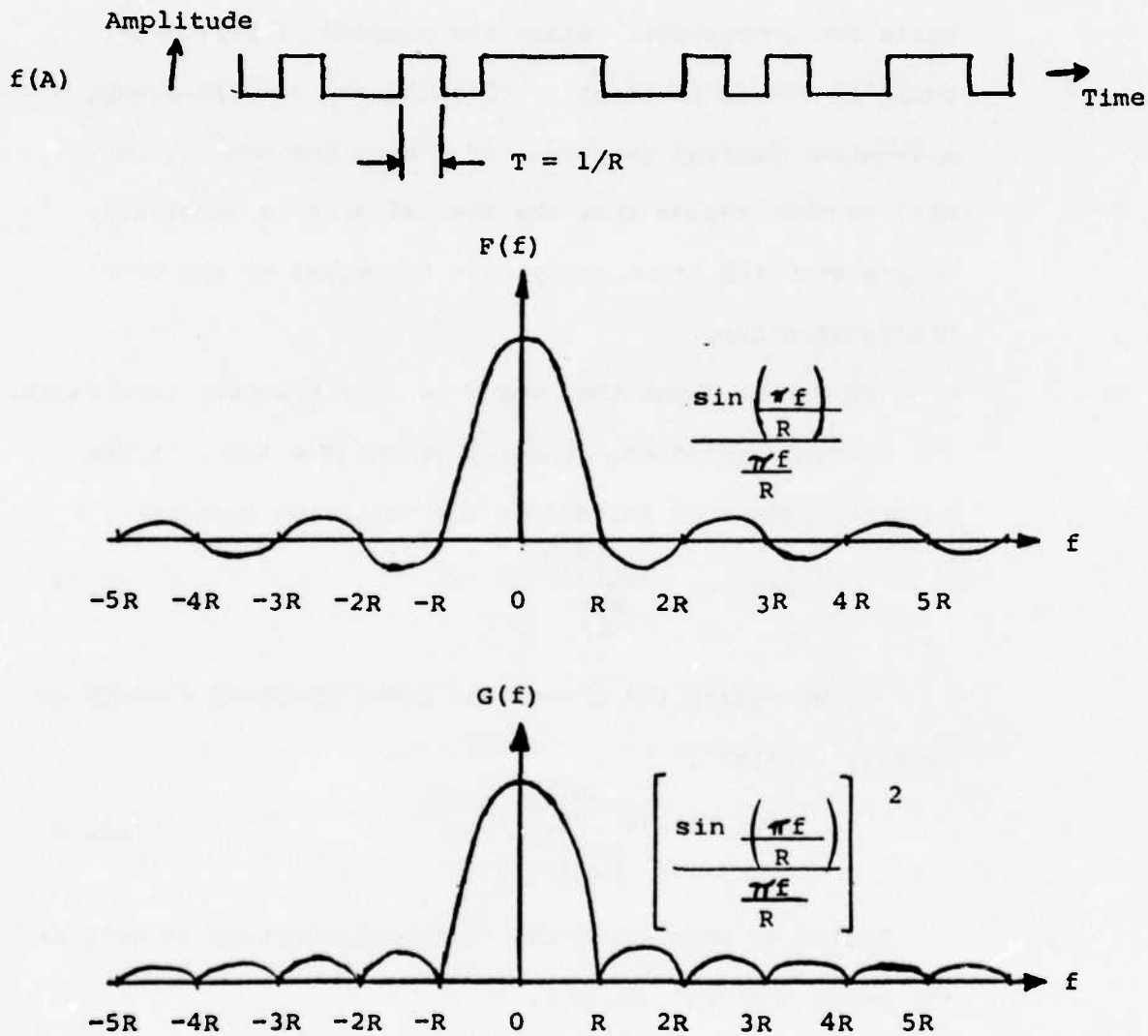


Figure 30. Random Data Spectrum

example is the spectrum analyzer. For this reason, a very convenient bandwidth measurement is the first null to first null ( $-R$  to  $R$ ) bandwidth.

Keeping the previous discussion in mind, plus the fact that the RF symbol rate for BPSK is  $R$  symbols/sec., while for QPSK and SQPSK the RF symbol rate is  $R/2$  symbols/second, one could readily ascertain that the spectral densities of the three forms of PSK are as shown in Figure 31. In this diagram  $F_c$  is the carrier frequency modulated by the data. From the figure one may easily describe the spectral occupancy of QPSK and SQPSK as only one half that of BPSK for the same digital data rate. Also, the null to null bandwidth is twice the RF symbol rate, which implies a bandwidth of  $2R$  Hz for the BPSK signal but only  $R$  Hz for the QPSK and SQPSK signals. This means that by using the orthogonal QPSK or SQPSK encoding systems one is able to transmit the same amount of information in one half of the bandwidth used by a BPSK encoding scheme.

The first null to first null bandwidth is also important in receiver IF stages as this is the bandwidth of the filters typically used in these stages to provide channel selectivity and to limit the broadband noise present at the receiver input. An integration of the power spectral density in the null to null bandwidth would show that 92% of the total energy of the modulated carrier spectrum is contained within

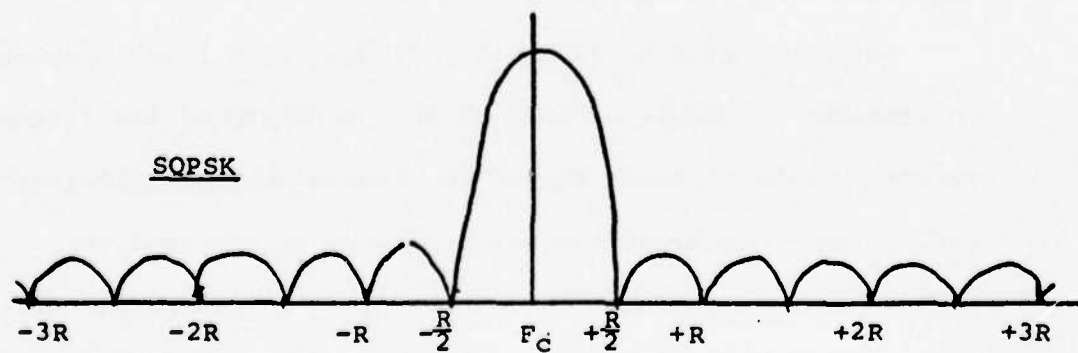
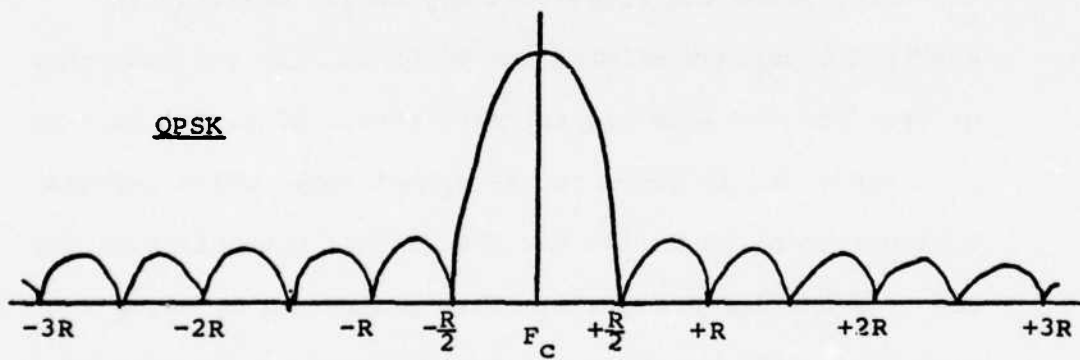
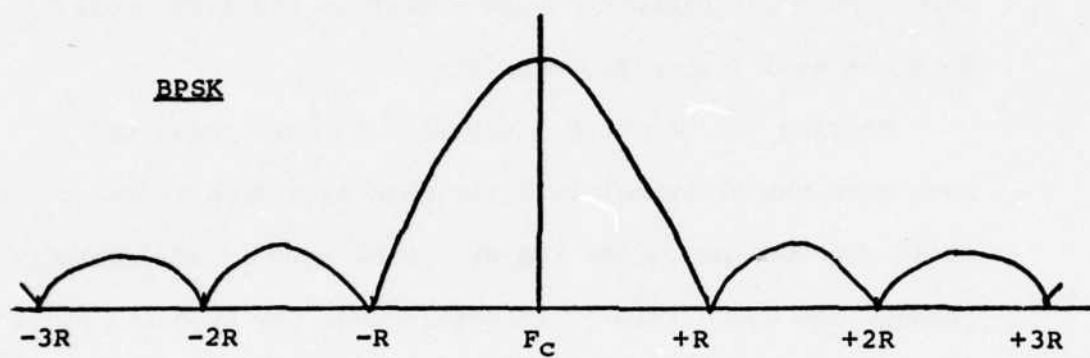


Figure 31. PSK Spectrums, Two and Four Phase

this bandwidth. Thus, a filter bandwidth of twice the RF symbol rate includes most of the signal energy but excludes noise and interference outside the signal bandwidth.

The major difference between QPSK and SQPSK has already been mentioned and is far more subtle than the spectral occupancy difference between the two phase and four phase forms of modulation just discussed. S.A. Rhodes has analytically detailed the difference between QPSK and SQPSK, which he calls offset QPSK modulation, so only the results of his analysis will be presented.<sup>1</sup>

Referring to Figure 32 one sees that the unfiltered QPSK and SQPSK data spectrums are the same, with the higher order sidebands decreasing in amplitude only very slowly. These sidebands produce interference at frequencies far away from the carrier where other channels are located. In the filtered version both QPSK and SQPSK are still the same but a single pole filter rolling off at  $F_c \pm R/2$  has been introduced. The effect of the additional attenuation outside of  $F_c \pm R/2$  is evidenced in the more rapid rolloff of the data spectrum sidebands. The final graph reveals the true difference between QPSK and SQPSK. Here, the signal has been filtered as shown in the second graph and then hard amplitude limited. The main lobe of signal energy shows little difference between the two signals, but the farther

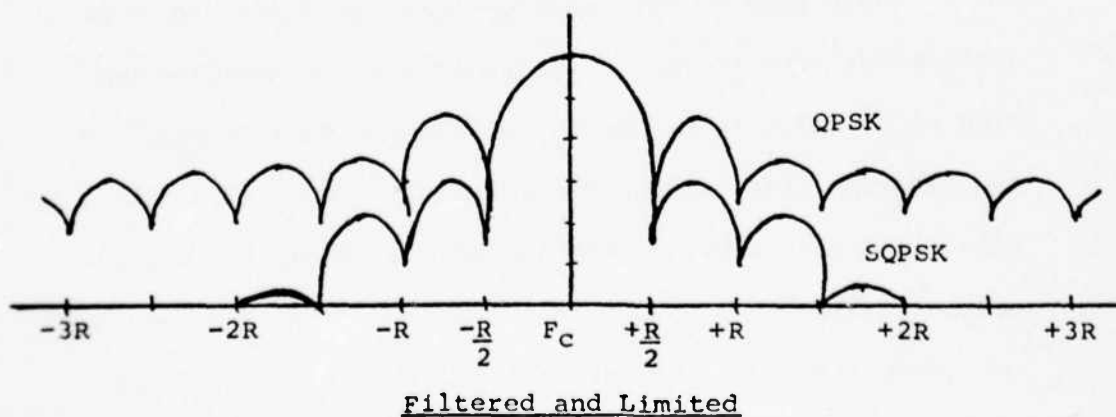
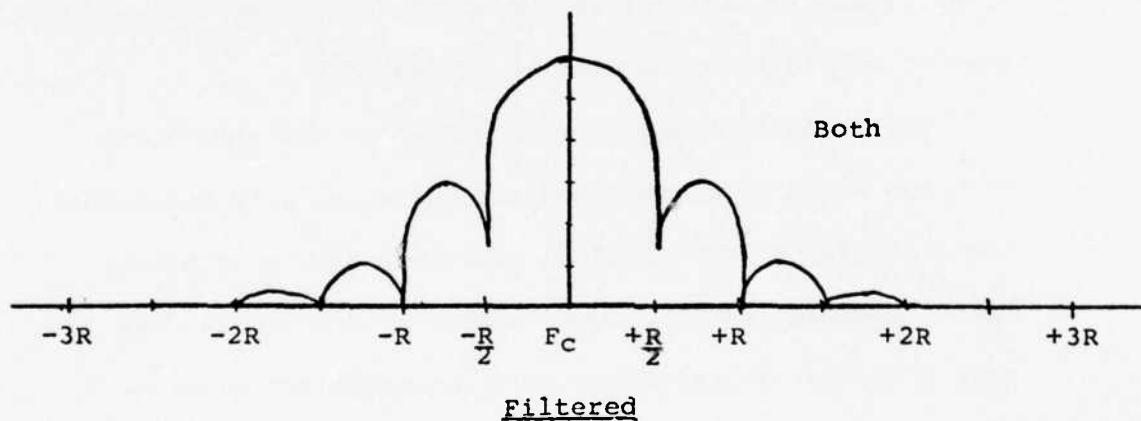
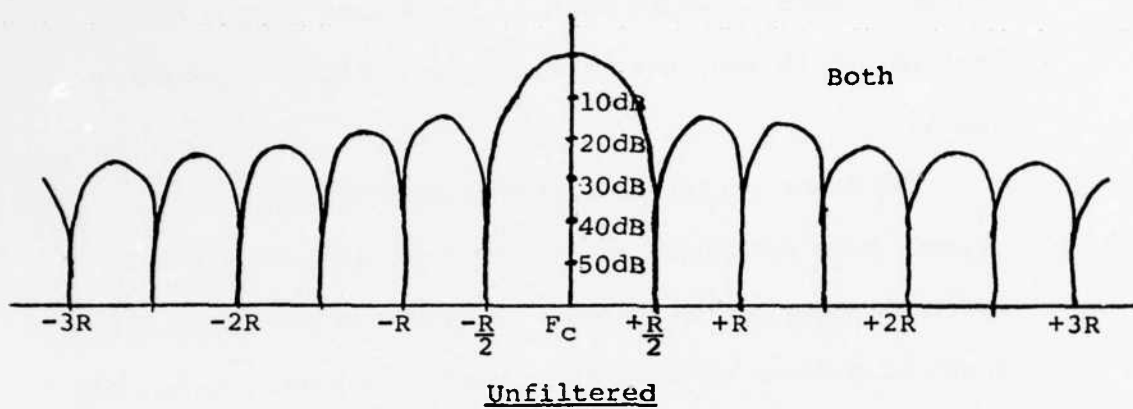


Figure 32. QPSK vs SQPSK, Unfiltered, Filtered, and Filtered and Limited

out one compares sidebands the greater is the difference. The QPSK spectrum sidebands have almost returned to the prefiltered, prelimiting level and the SQPSK sidebands have remained approximately at the filtered level. The large reduction in energy far away from the carrier frequency allows lower level channels at these frequencies, as well as permitting other channels to be placed closer to the carrier, and thus increasing the total number of channels by decreasing the channel to channel spacing.

The last comparison of the three modulation methods is how much signal power is required in the presence of a noisy channel to achieve a specified probability of error for a data bit. Without derivation, the probability of error equation for coherent detection of BPSK signals is:

$$P_e = \frac{1}{2} \operatorname{erfc} \sqrt{\text{SNR}} \quad \text{EQ. 4}$$

Where:  $P_e$  = Probability of error of a data bit

$\operatorname{erfc}$  = Complementary error function

SNR = Signal to noise ratio at detector input

An ideal detector uses optimum data filtering so the SNR is usually defined as the energy per bit divided by the noise power in a one hertz bandwidth.

$$E_b = \frac{S}{R} = \frac{\text{Signal Power}}{\text{Bit Rate}} \quad \text{EQ. 5}$$

$N_o$  = Noise power in a 1 Hz bandwidth

Thus, the ideal BPSK bit error is defined by:

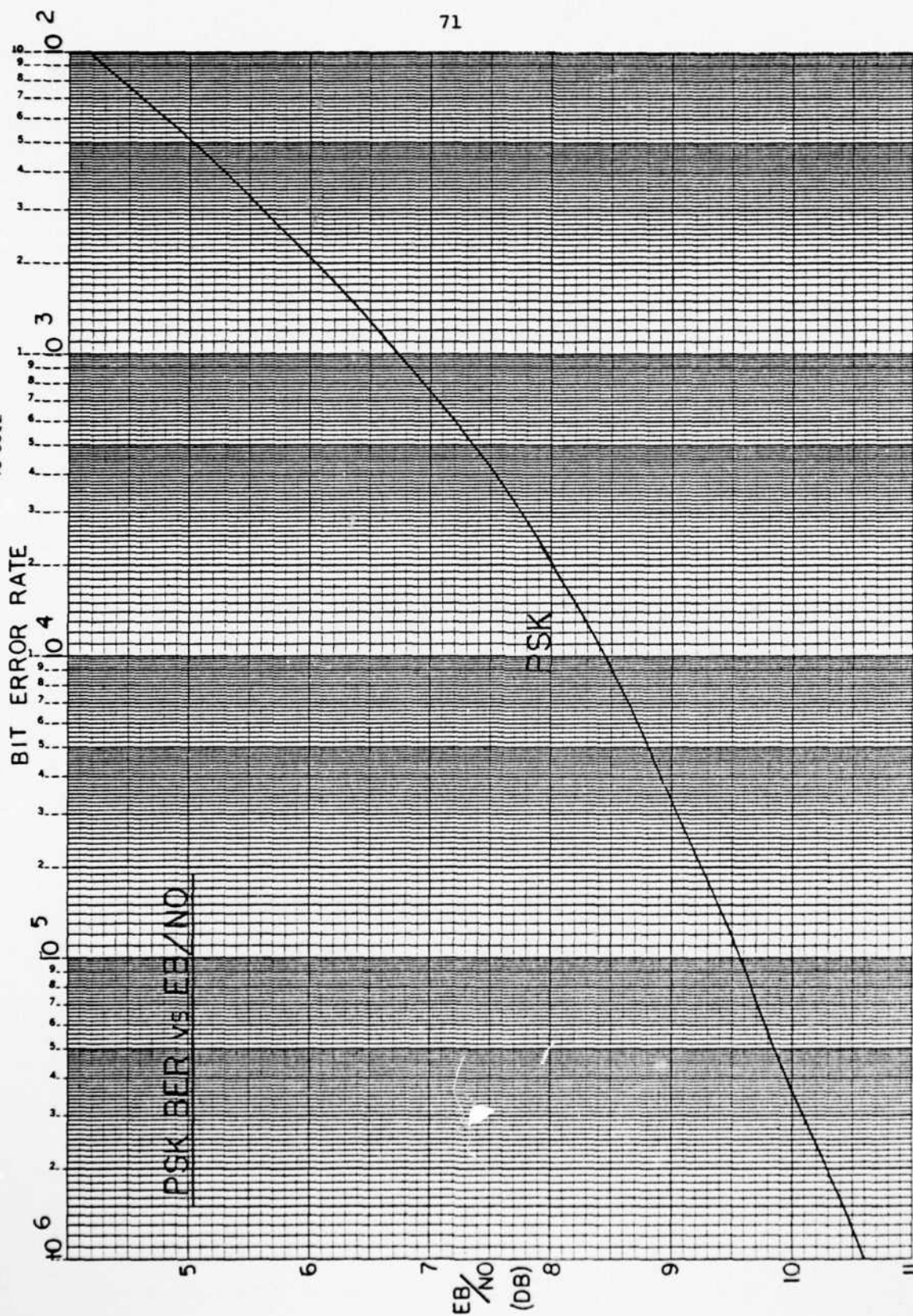
$$P_e = \frac{1}{2} \operatorname{erfc} \sqrt{E_b/N_o} \quad \text{EQ. 6}$$

For QPSK and SQPSK recall that each of the four phase orthogonal modulation schemes may be decomposed into two BPSK systems operating at half the digital data rate. The four phase schemes may then be compared to BPSK for bit error rate in a somewhat heuristic manner. Each component of the four phase systems has half of the total power of the signal contained within itself but the symbol rate of each orthogonal component is one half of the data rate so that each symbol is twice as long as a data bit. Thus, we may calculate the energy per symbol of the I or Q channel.

$$E_s = \frac{(S/2)}{(R/2)} = \frac{S}{R} = E_b \quad \text{EQ. 7}$$

The energy per symbol is exactly equal to the energy per bit of the BPSK system. Since half of the information is transmitted over the I channel and half over the Q channel, and a one-to-one correlation exists between the symbols and bits, all of the information is transmitted with the same energy per bit as BPSK. Thus, the error rates of BPSK, QPSK, and SQPSK are identical as defined by EQ. 6. Figure 33 graphically presents equation 6.

The only modification to the theoretical BER usually occurs in the process of ambiguity resolution. Figure 23 shows a transmitter and receiver communicating over a noisy medium with both having knowledge of exactly where  $0^\circ$  phase lies. In reality, the receiver would be situated far away

Figure 33. PSK BER vs.  $E_b/N_0$

from the transmitter and only have the modulated carrier for information. The receiver is capable of deriving a pseudo carrier from the received signal for comparison with the incoming modulation but this derived reference may be  $0^\circ$  or  $180^\circ$  for BPSK; and,  $0^\circ$ ,  $90^\circ$ ,  $180^\circ$ , or  $270^\circ$  for the QPSK and SQPSK signals.

To resolve this ambiguity one could send a reference code periodically so the receiver could correct its reference to  $0^\circ$  but this would lower the information rate as data could not be sent during the reference code transmission. An alternative method more usually employed is the use of difference encoding the data so that information is contained in the phase change from one symbol to the next. The name for this method of ambiguity resolution is Differentially Encoded Phase Shift Keying, or DEPSK. Figure 34 illustrates the information encoding of PSK and DEPSK.

Notice in PSK that if  $\phi_{i+1}$  were incorrectly estimated, the only error occurring would be a wrong  $M_{i+1}$ . A one to one correspondence exists between phase estimation errors and symbol errors. DEPSK has a slightly different decoding situation, however. An error in estimating  $\phi_{i+1}$  would lead to an error in  $\phi_{i+1}$  and  $\phi_{i+2}$ . Thus, two errors would be generated by DEPSK for each phase estimation error, and this is the penalty paid for this form of ambiguity resolution. Figure 14 plots the bit error rate of PSK & DEPSK vs.  $E_b/N_0$  for

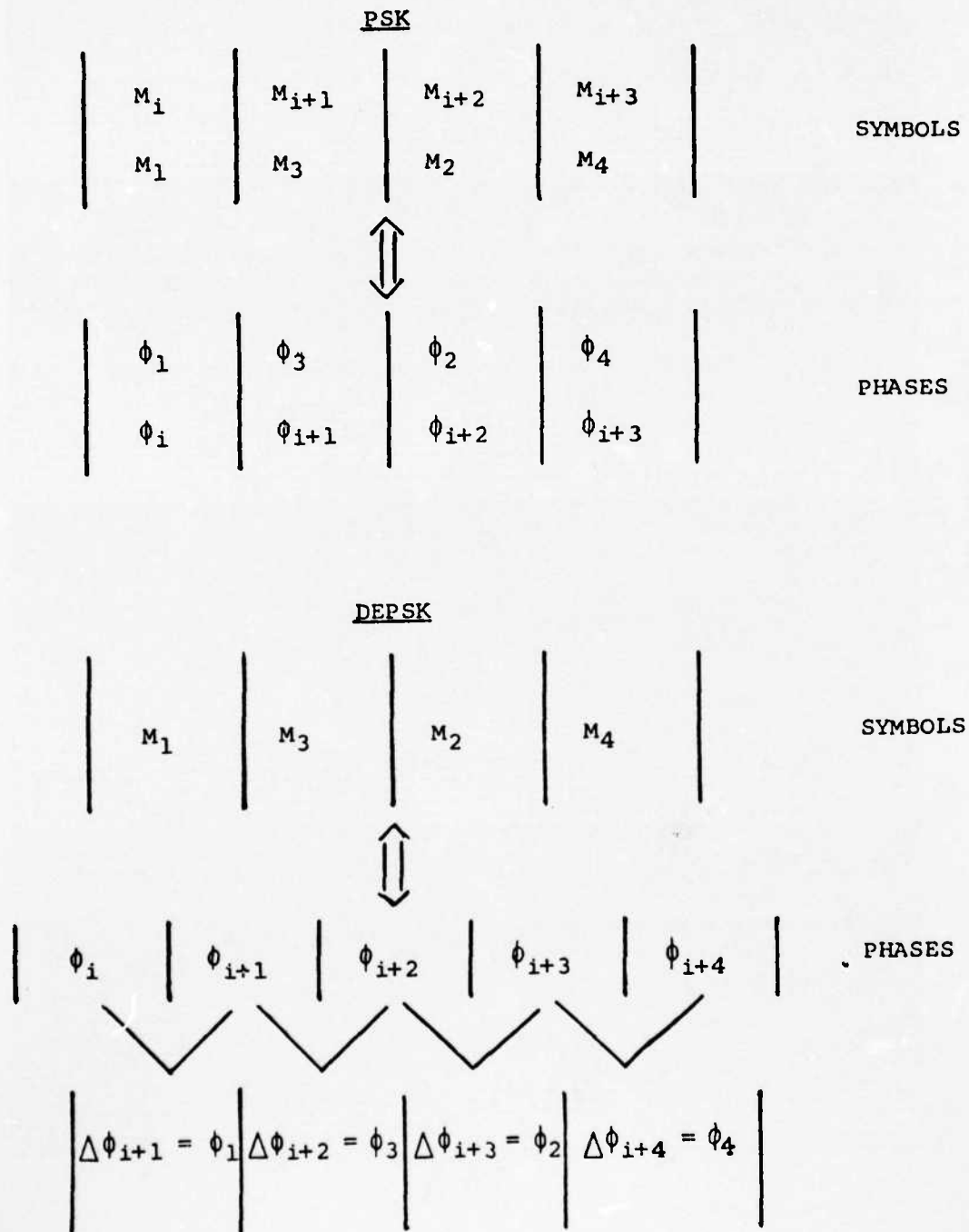
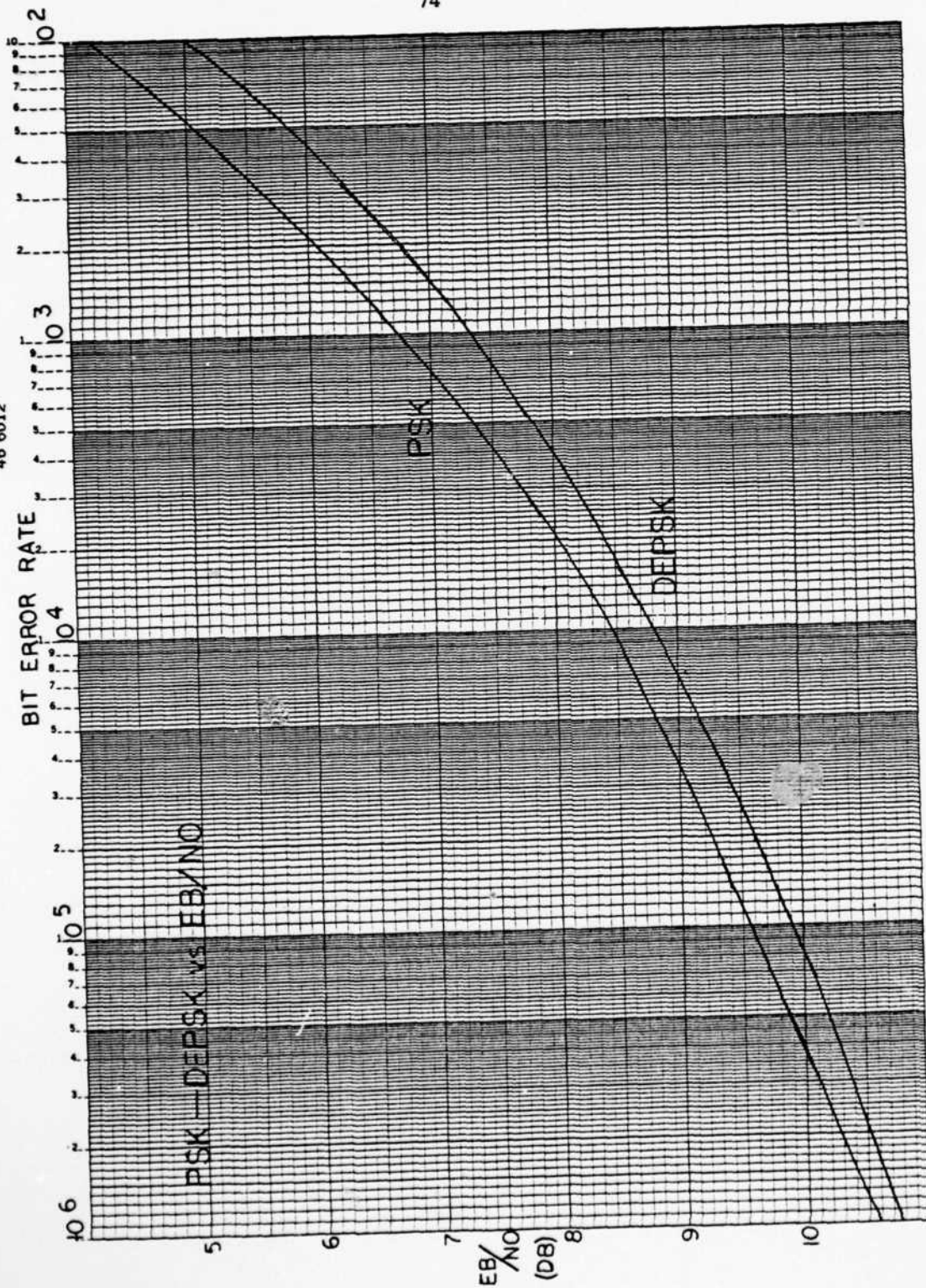


Figure 34. PSK vs. DEPSK - Encoding

Figure 35. PSK-DEPSK vs.  $E_b/N_0$

comparison purposes. The increase in signal power required to achieve the same BER performance as PSK at  $10^{-5}$  BER is only .3 dB, a relatively small price to pay for ambiguity resolution.

A summary of this section is presented in Table 1 for quick comparison of BPSK, QPSK, and SQPSK.

TABLE 1. COMPARISON OF BPSK, QPSK, AND SQPSK

PARAMETER	BPSK	QPSK	SQPSK
Data Rate - Bits/Sec.	R	R	R
RF Symbol Rate - Symbol/Sec.	R	R/2	R/2
1st Null to 1st Null Bandwidth	2R	R	R
Post Limiting Sidebands	Present	Present	Absent
Maximum Instantaneous Phase Change	180°	180°	90°
Eb/No for $10^{-5}$ BER - dB	+9.8	+9.8	+9.8

### 2.1.3 Generating and Detecting PSK

#### 2.1.3.1 Generation

Since PSK is a form of angle modulation one needs a device which modifies the phase angle of a CW carrier according to the desired information. The simplest phase modification possible is  $180^\circ$ , or inversion of the signal carrier, and thus most modulators use one or more phase inverters. Some of the most common devices used are:

- (1) Double Balanced Mixers - (Diodes and Transformers)
- (2) Differential Amplifiers
- (3) Multipliers - (Analog or Digital)

The use of these devices for BPSK generation is straightforward as shown in Figure 36. A digital control line selects  $0^\circ$  or  $180^\circ$  transmission of the carrier frequency according to the signal present at the data input.

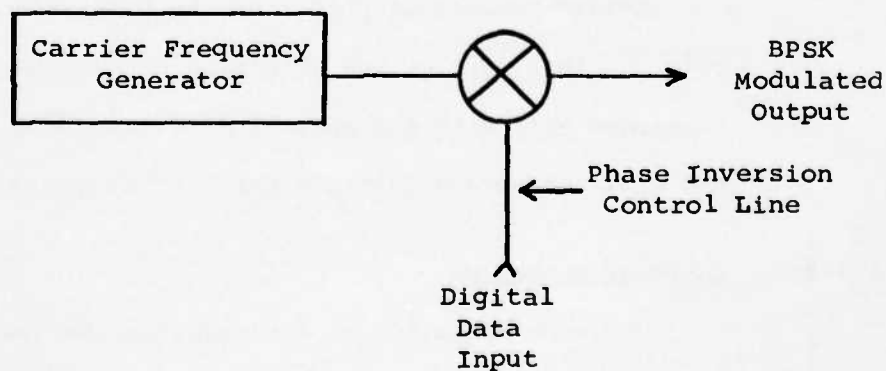


Figure 36. BPSK Generation

To use phase inversion switches for generating four phase PSK such as QPSK and SQPSK, it is necessary to generate the quadrature component of the carrier frequency for the second data stream to modulate. As shown in Figure 37, the input data stream is split in half, thus halving the data rate in I and Q channels. If desired difference encoding is performed at this point to eliminate phase ambiguity at the receiver. The carrier frequency is split into I and Q channels which are  $90^\circ$  out of phase by a phase shifting network such as a  $90^\circ$  hybrid coupler or an LC network. The I and Q data each modulate their respective channels which are then summed together to form the four phase modulated output. The only difference between QPSK and SQPSK is that the I and Q outputs of the data splitter change simultaneously for QPSK, whereas the I and Q outputs change at different, i.e. non-coincident times for SQPSK.

Larger numbers of phases can be generated by extrapolating this same method to N bits or M phases, but we are concerned only with two phase and four phase generation here and will not pursue Multiple Phase Shift Keying, or MPSK.

#### 2.1.3.2 Coherent Detection

Coherent detection of PSK requires the use of a phase sensitive device to compare the phase of an incoming modulated carrier with a carrier phase reference. Generally, the

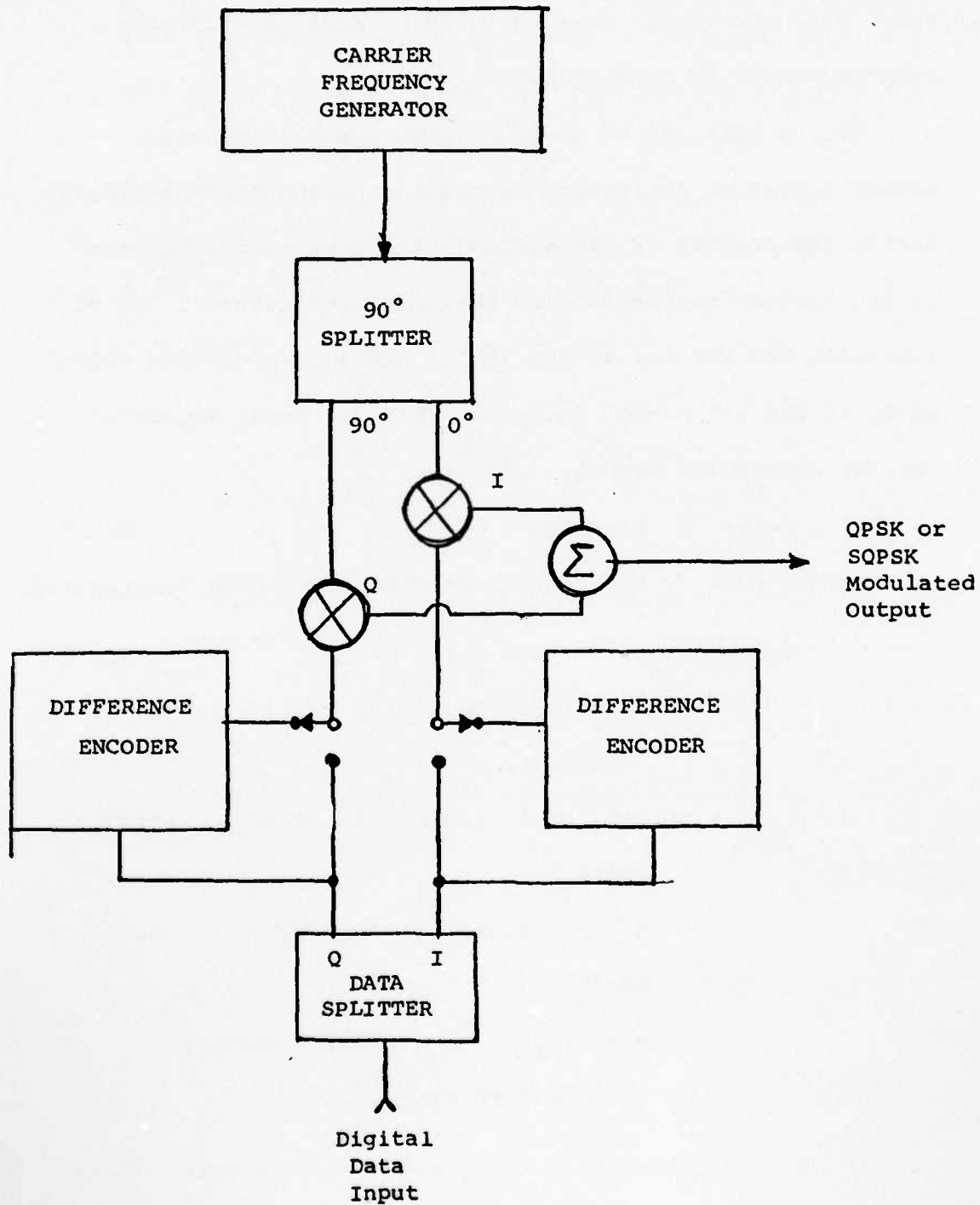


Figure 37. QPSK and SQPSK Generation

devices that are useful for generating a PSK modulated carrier are also useful for demodulating a carrier, and hence PSK detection. Some of these devices have already been mentioned in Section 2.1.3.1.

Noting that all of these devices are multipliers, either linear or nonlinear, one would attempt to analytically derive the process of PSK demodulation from multiplication of the carrier reference with the modulated carrier. If we represent the carrier as  $\sin(\omega_c t)$  and the modulation symbol as  $\theta_i$  in the  $i$ th symbol interval, then the total modulated carrier expression becomes:

$$f_1(t) = \sin(\omega_c t + \theta_i) \quad \text{EQ. 8}$$

Multiplying by the carrier reference and then rearranging:

$$\begin{aligned} f_2(t) &= \sin(\omega_c t + \theta_i) \sin(\omega_c t) & \text{EQ. 9} \\ &= \left[ \sin(\omega_c t) \cos(\theta_i) + \cos(\omega_c t) \sin(\theta_i) \right] \sin(\omega_c t) \\ &= \sin^2(\omega_c t) \cos(\theta_i) + \cos(\omega_c t) \sin(\omega_c t) \sin(\theta_i) \\ &= \frac{1}{2} \left[ 1 - \cos(2\omega_c t) \right] \cos(\theta_i) + \frac{1}{2} \sin(2\omega_c t) \sin(\theta_i) \\ &= \frac{1}{2} \cos(\theta_i) - \frac{1}{2} \cos(2\omega_c t) \cos(\theta_i) + \frac{1}{2} \sin(2\omega_c t) \sin(\theta_i) \end{aligned}$$

If we next filter  $f_2(t)$  with a low pass function which cuts off below the carrier frequency  $\omega_c$ , only one term

remains in the expression for  $f_2(t)$ . The higher frequency terms appearing at twice the carrier frequency,  $2\omega_c$ , are rejected by this filter and the result is:

$$f_3(t) = \frac{1}{2} \cos(\theta_i) \quad \text{EQ. 10}$$

We see that  $f_3(t)$  is a time invariant transcendental representation of  $\theta_i$ , the transmitted phase symbol. Note that there are two possible phases which would give the same  $f_3(t)$  since our equation was only for one channel or BPSK. A second orthogonal channel could be added which would not influence the data in this channel whatsoever, and that second channel data could be obtained by multiplying the modulated carrier by  $\cos(\omega_c t)$  instead of  $\sin(\omega_c t)$ . This realization leads us to believe that we can now demodulate QPSK by reversing the modulation process just as in BPSK. Figure 38 shows the basic demodulation process for BPSK and QPSK.

#### 2.1.3.3 Data Detection

Extracting symbol or bit information from  $f_3(t)$  becomes more complicated when the signal has been corrupted with noise. During time  $t_i$  symbol phase  $\theta_i$  is transmitted but the noise present makes the received phase vary randomly about  $\theta_i$ . One would guess that a best estimation of  $\theta_i$  could be obtained by averaging the received phase during time  $t_i$ , and this turns out to be approximately true. An optimum detector does just that by performing the following function.

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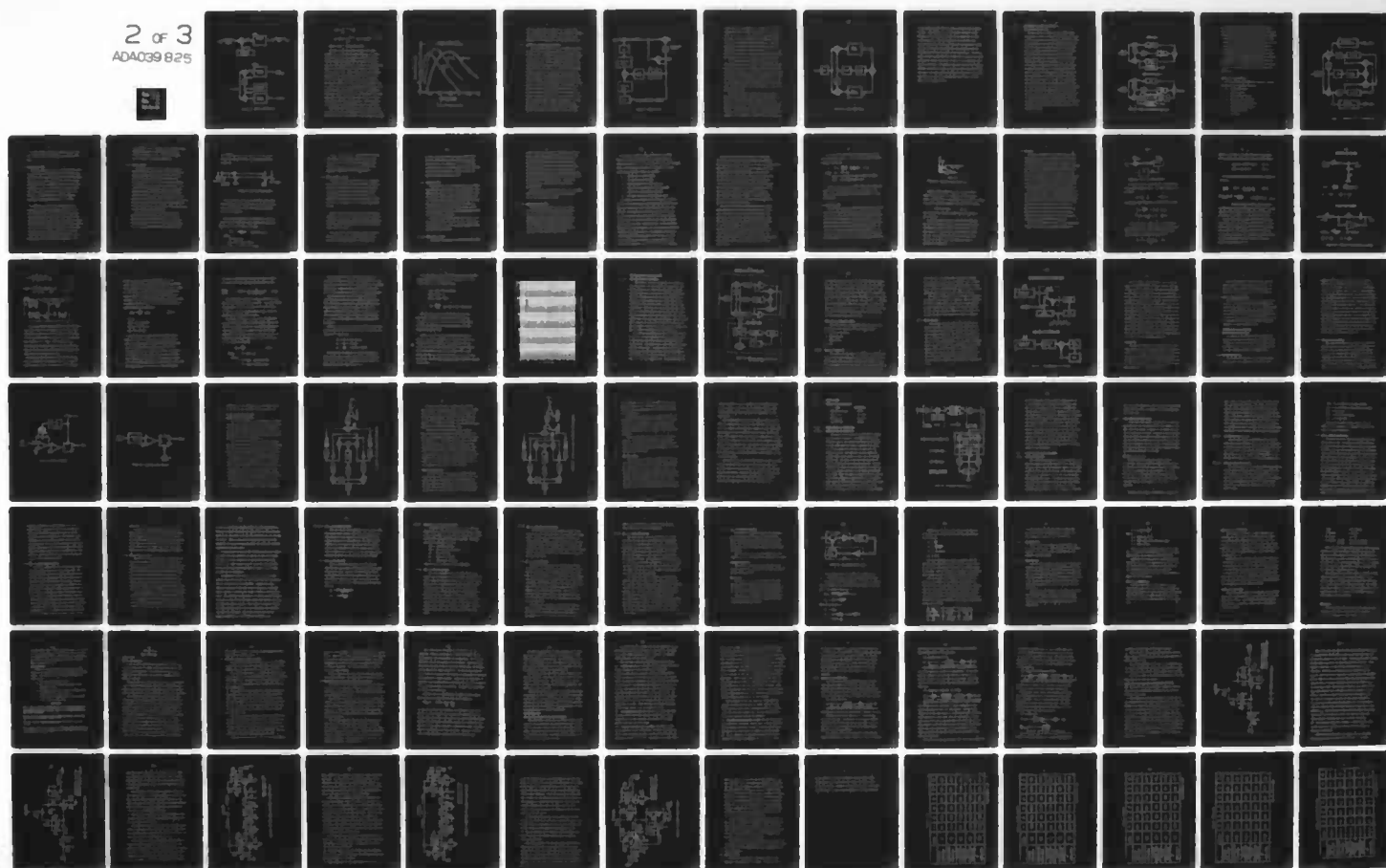
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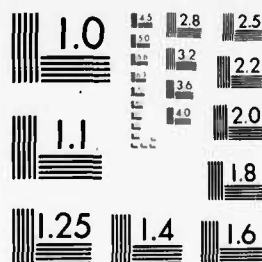
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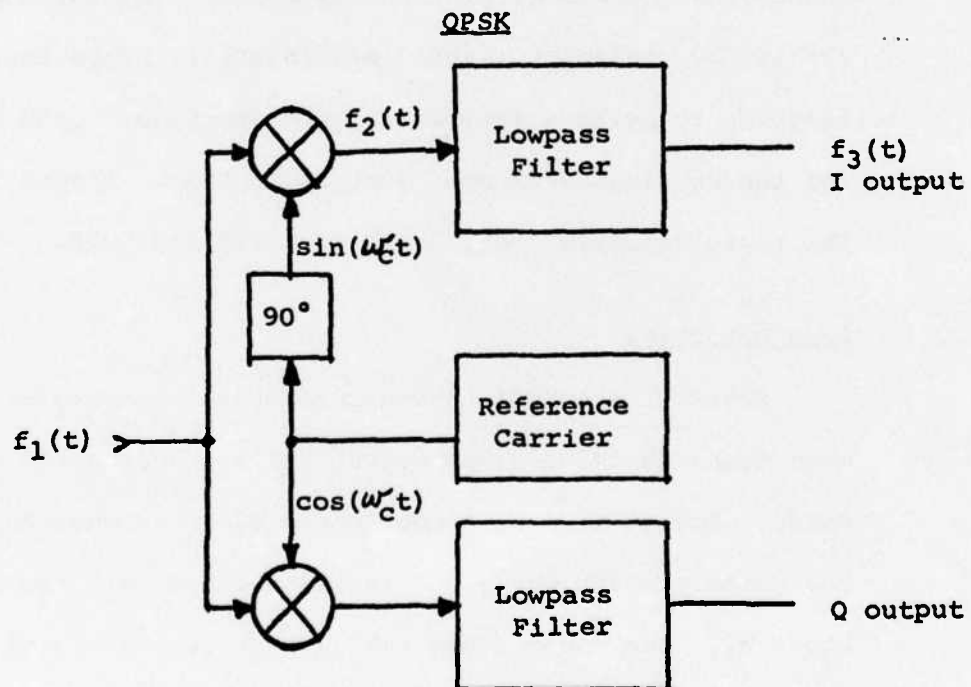
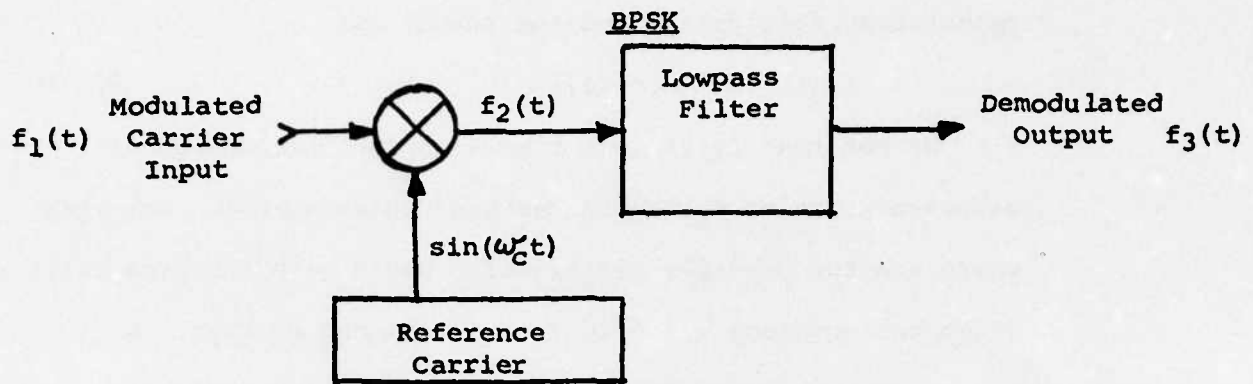


Figure 38. Coherent Demodulation

$$f_4(t) = \int_{t_1}^{t_{i+1}} f_3(t) dt$$

$$\theta_i + \hat{\theta}_n(t) = \int_{t_1}^{t_{i+1}} [\theta_i + \theta_n(t)] dt \quad \text{EQ. 11}$$

Where:  $\theta_n(t)$  = Random Phase Noise

Integration over the symbol interval is the best estimate one can make for the symbol phase  $\theta_i$ . All other methods of estimation will yield more inaccurate results than the integration method, which is called an optimum detector. Most other estimation methods use low pass filters whose cutoff frequency is of the same order as the symbol rate or slightly less. These filters perform an imperfect averaging of the received phase during time  $t_i$  and also include some energy from the previous time  $t_{i-1}$  usually. The imperfect average during  $t_i$  as well as the residue from  $t_{i-1}$  lead to more errors in estimating phase  $\theta_i$  with low pass filters than with the integration method. The degradation attributed to these filters usually is expressed in the extra signal power required to achieve a BER equivalent to that obtainable with an integrating detector. This degradation is equivalent to a loss in  $E_b/N_0$  or signal to noise ratio.

The degradation from several types of low pass filters as a function of cutoff frequency is shown in Figure 39.<sup>2</sup> The horizontal line at 0 dB degradation is the optimum integrating

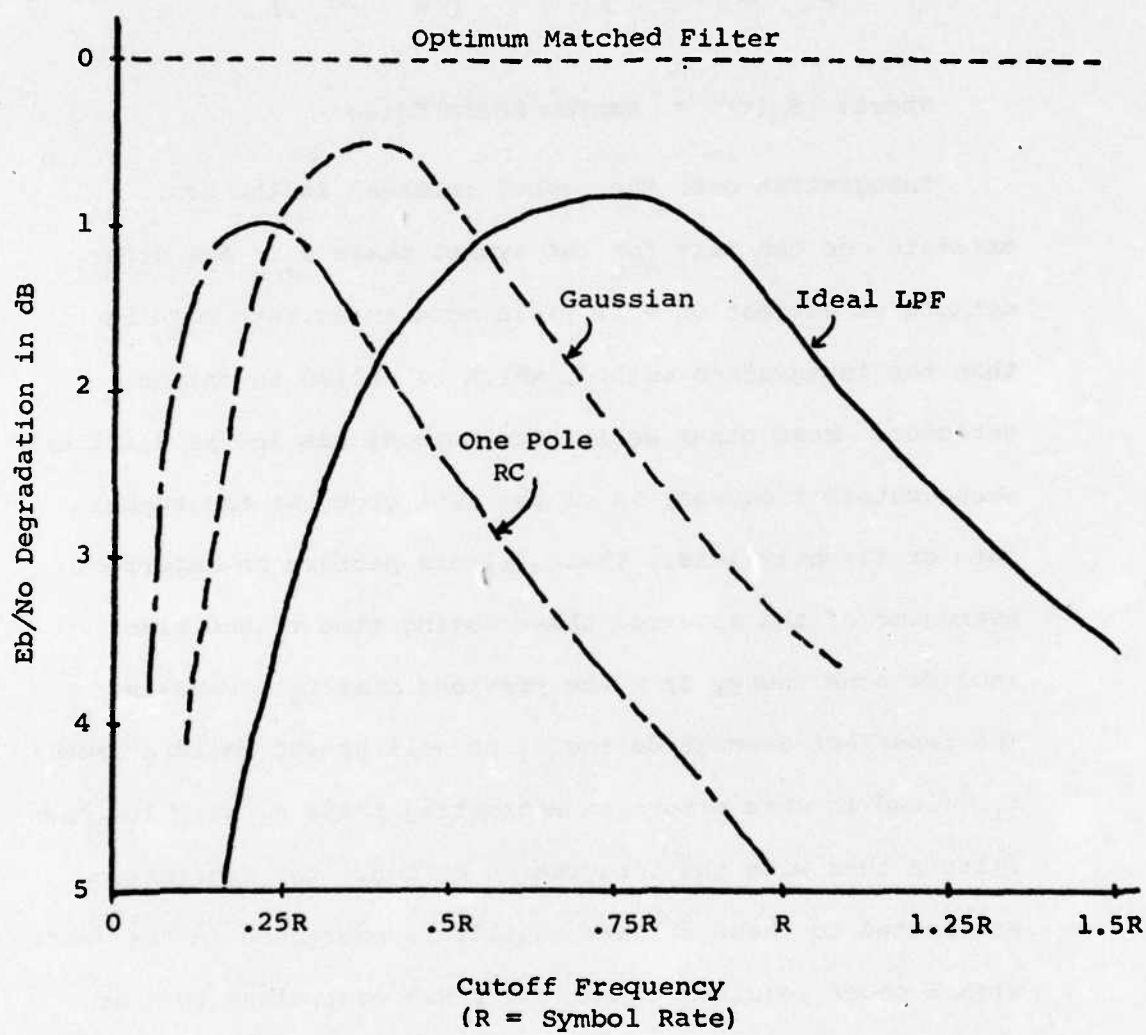


Figure 39. Data Filtering

detector. Notice that all other curves lie below this line, indicating worse performance. The performance degradation of these filters is usually traded off against the additional circuit complexity of the integrating detector.

#### 2.1.3.4 Providing A Coherent Carrier Estimate

As determined in Section 2.1.3.2 on coherent detection a coherent carrier reference is required in the demodulation process for PSK. Providing this carrier reference is usually a major portion of a complete demodulator and deserves considerable attention. One of two methods is normally used to derive a carrier reference, either the squaring loop or the data aided loop. The squaring loop multiplies the frequency modulated carrier by  $M$  in a nonlinear device, filters the resulting frequency and compares this with the phase of the carrier reference. Multiplication by  $M$  strips the data from the signal and leaves an unmodulated carrier. Figure 40 shows the block diagram of a squaring loop. Note that both the carrier reference and the incoming modulated carrier are multiplied by  $M$  so that both will be at the same final frequency. This allows the use of a mixer or multiplier to compare the reference and the incoming carrier phase. The loop filter is used to average the phase comparisons over an extended period of time so that a better carrier reference estimate can be made in the presence of noise. The loop

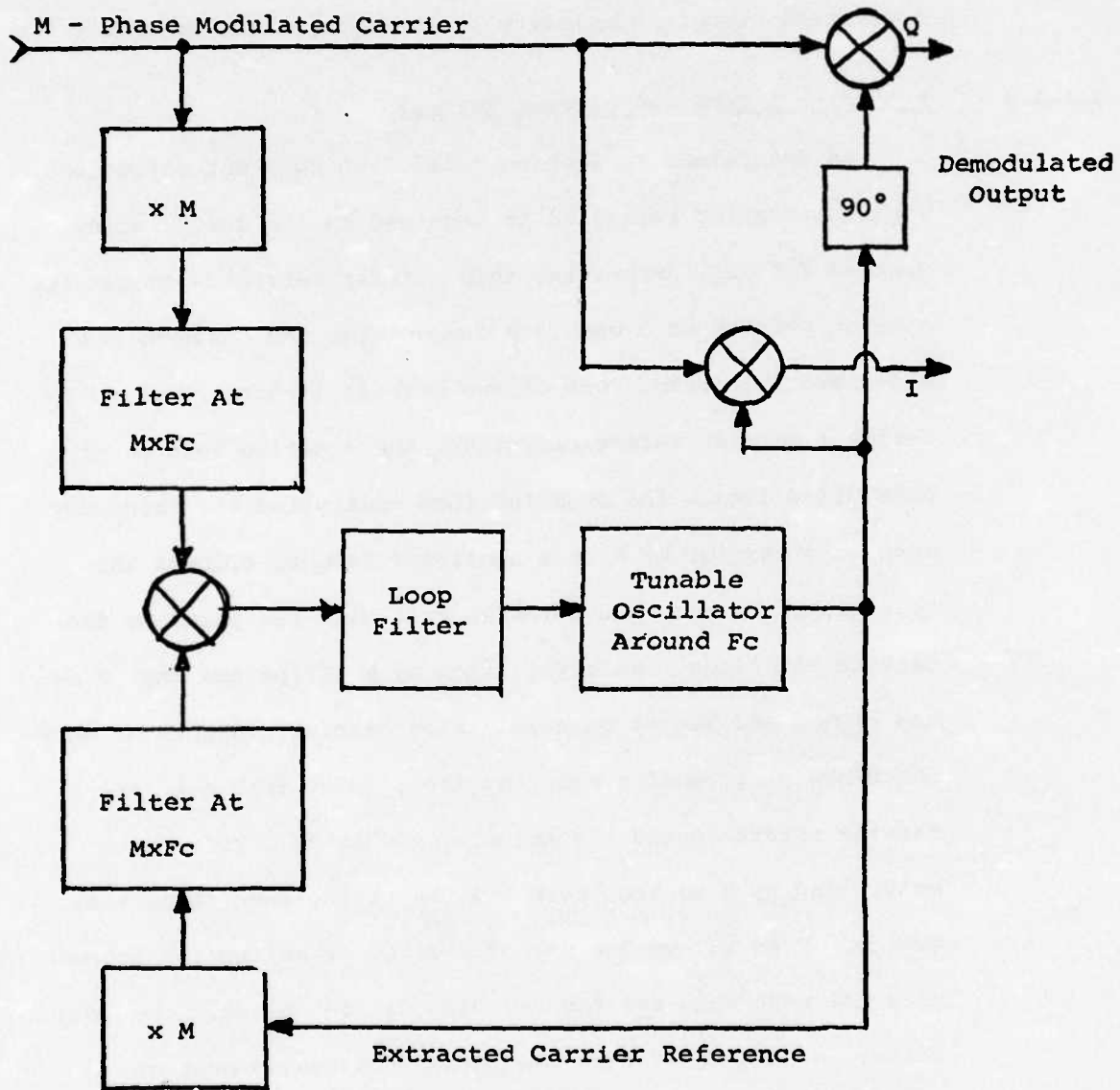


Figure 40. Squaring Loop

filter will not only determine the accuracy of the carrier estimate but also is chosen so as to have a stable carrier loop. An incorrect choice could cause oscillations within the loop. The major disadvantage of the squaring loop occurs in the use of nonlinear frequency multipliers. These devices exhibit poor efficiencies and also degrade the signal to noise ratio considerably. The only way to recover the lost signal to noise ratio is modifying the loop filter by making it narrower and this is not always possible or desirable.

The second method of extracting a carrier reference from a modulated carrier is called a data-aided loop because the data itself is used to modify the tuning information for the reference oscillator. As the data is used in reconstructing a carrier reference there is no large degradation in SNR as when the data is stripped away by multipliers. This is the main advantage of the data-aided loop over the squaring loop. The most common form of data-aided loop in use is the modified Costas loop.

The block diagram for a data-aided loop is shown in Figure 41. The specific case shown is a BPSK decoder, but note that two mixers are used to generate an I and a Q channel just as in QPSK. The I channel is aligned in phase with the incoming carrier whereas the Q channel is  $90^\circ$  out of phase with the incoming carrier. As a result random data appears at the I output as  $\pm 1$  (normalized) and 0 appears at

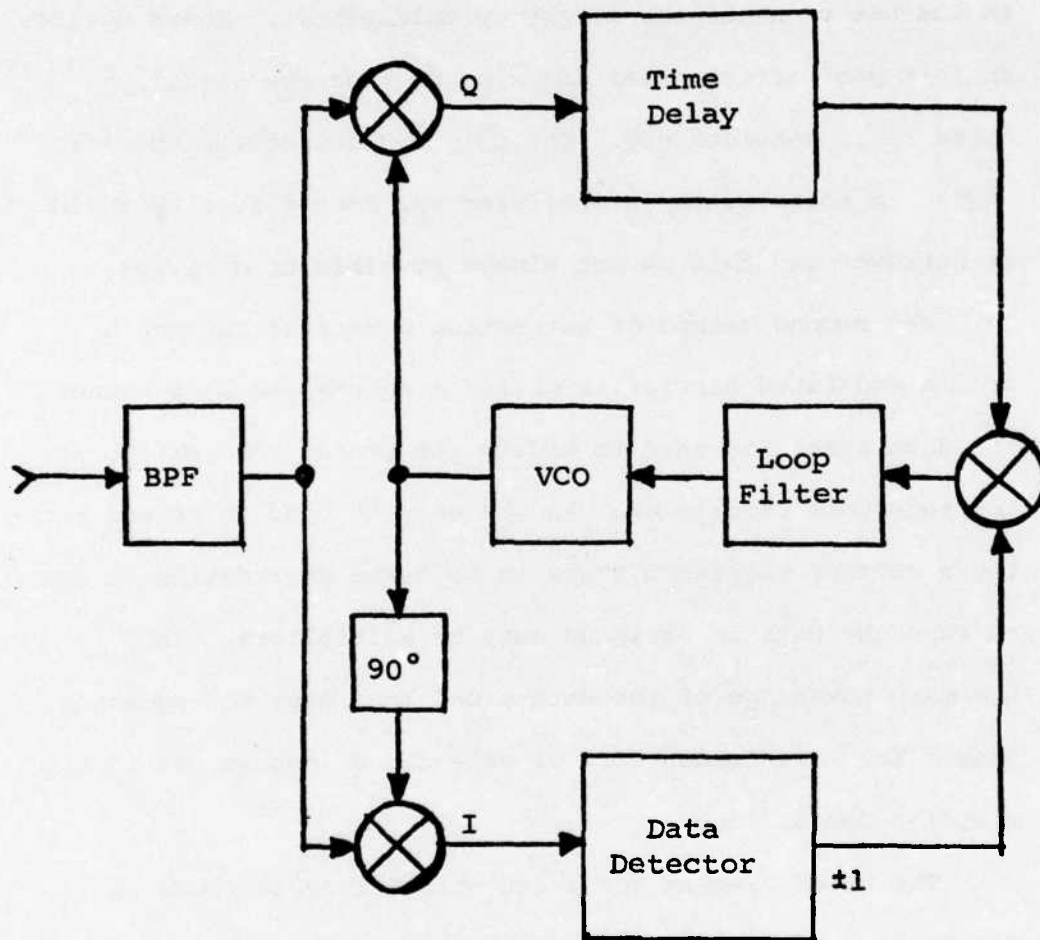


Figure 41. Data Aided Loop

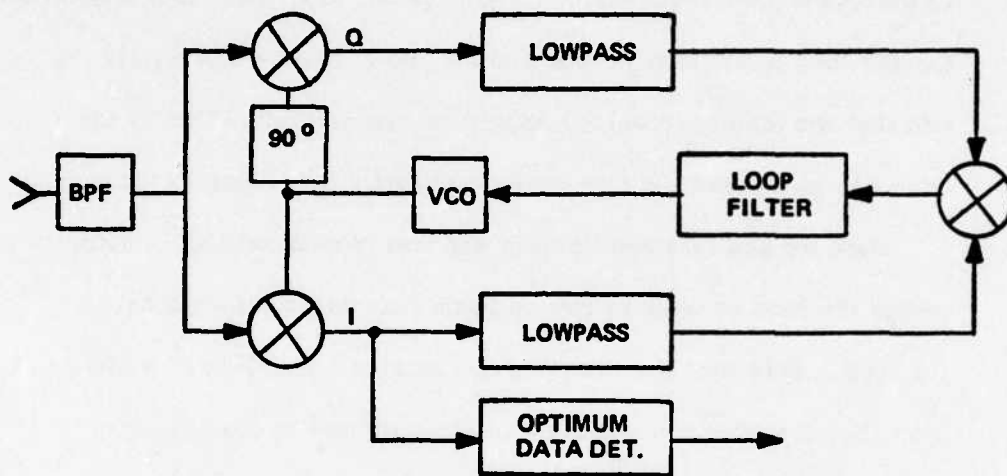
the Q channel output when the loop is locked to an incoming carrier. The transmission of the signal through a noisy medium will give rise to additive noise appearing in both I and Q channels. The data detector will estimate the digital data as  $\pm 1$  over a time interval and send this output to the "third mixer" to modify the time delayed Q channel information before it is sent to the loop filter. The third mixer is what enables the data-aided loop to utilize the data information rather than throw it away as in a nonlinear frequency multiplier. By changing the loop sensitivity to phase changes from plus to minus in accordance with the data detector output the data-aided loop exactly cancels out the incoming modulation and makes the VCO and loop filter see what appears to be a CW carrier.

## 2.1.4 Implementation of a Modified Costas Loop

### 2.1.4.1 Block Diagram and Description

The block diagrams of a Costas loop and a modified Costas loop are shown in Figure 42. Note that while the regular Costas loop is merely a low pass version of a squaring loop, the modified Costas loop is a non-optimum data aided loop. Referring back to Figure 41 we see that an optimum data detector is included in the ideal data aided loop, whereas the modified Costas loop has a non-optimum data detector in the carrier loop and an optimum data detector external to the carrier loop. The reason for this is the time delay required in the Q channel of a true data aided loop. This delay is very difficult to implement at low bit rates in an analog system. The delay required is equal to the time it takes the optimum data detector to decide which symbol was sent and this is usually equal to one symbol length. In the modified Costas loop a hard limiter with no time delay decides the symbol being sent instantaneously and multiplies the Q output in the third mixer on a real time basis rather than a delayed basis. The two low pass filters will have equal time delay if they are of the same implementation type and cutoff frequency, and thus the two signals arriving at the third mixer will be time coincident as required in the data aided loop. All further discussion will be in reference to the modified Costas loop. Further, the discussion will be restricted to an analog implementation of the modified Costas loop.

## COSTAS LOOP



## MODIFIED COSTAS LOOP

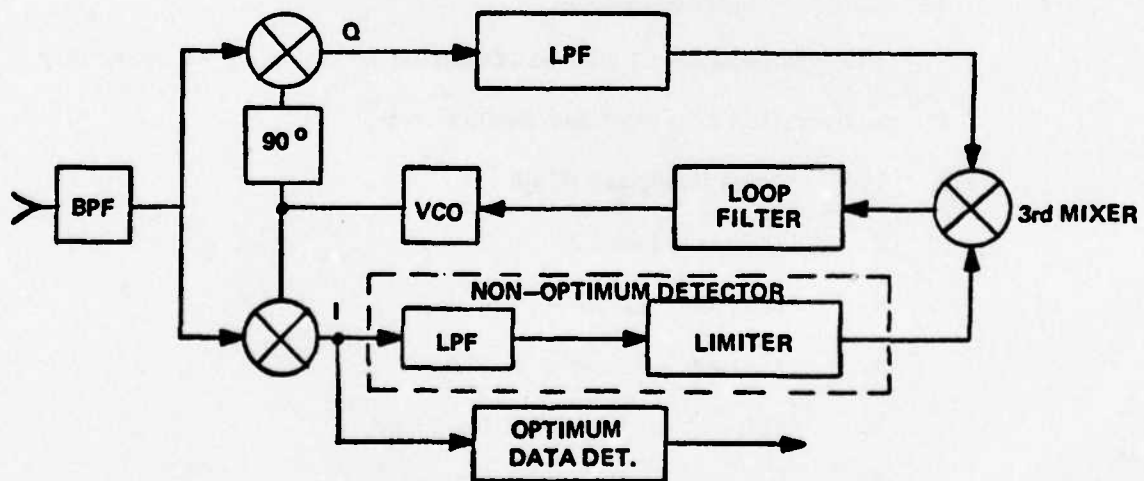


Figure 42. Costas Loop and Modified Costas Loop

The modified Costas loop in Figure 42 is accurate for BPSK only, and we also wish to demodulate QPSK and SQPSK. In each of these four phase systems data would be present in both the I and Q channels so the block diagram in Figure 42 would not be useful. Since data is present in both channels one would be led to suspect that a modified Costas loop would have to treat both I and Q channels similarly and that the diagram topology should be symmetrical. This is the case and in Figure 43 a four phase modified Costas loop is shown.

Here we see that two limiters and two third mixers are employed within the loop as well as two optimum data detectors external to the loop. Note that the channels are labeled I and Q as in a biphase loop, but that this nomenclature is arbitrary due to the symmetry of the loop.

#### 2.1.4.2 Discussion of Specific Blocks

The following items may be identified in Figure 43 as necessary for the operation of a modified Costas loop.

1. Input bandpass filter
2. Mixers - I and Q
3. Low pass filters - I and Q
4. Limiters - I (and Q for QPSK)
5. Third Mixers I (and Q for QPSK)
6. Voltage controlled oscillator
7. Phase shifter -  $90^\circ$
8. Loop filter

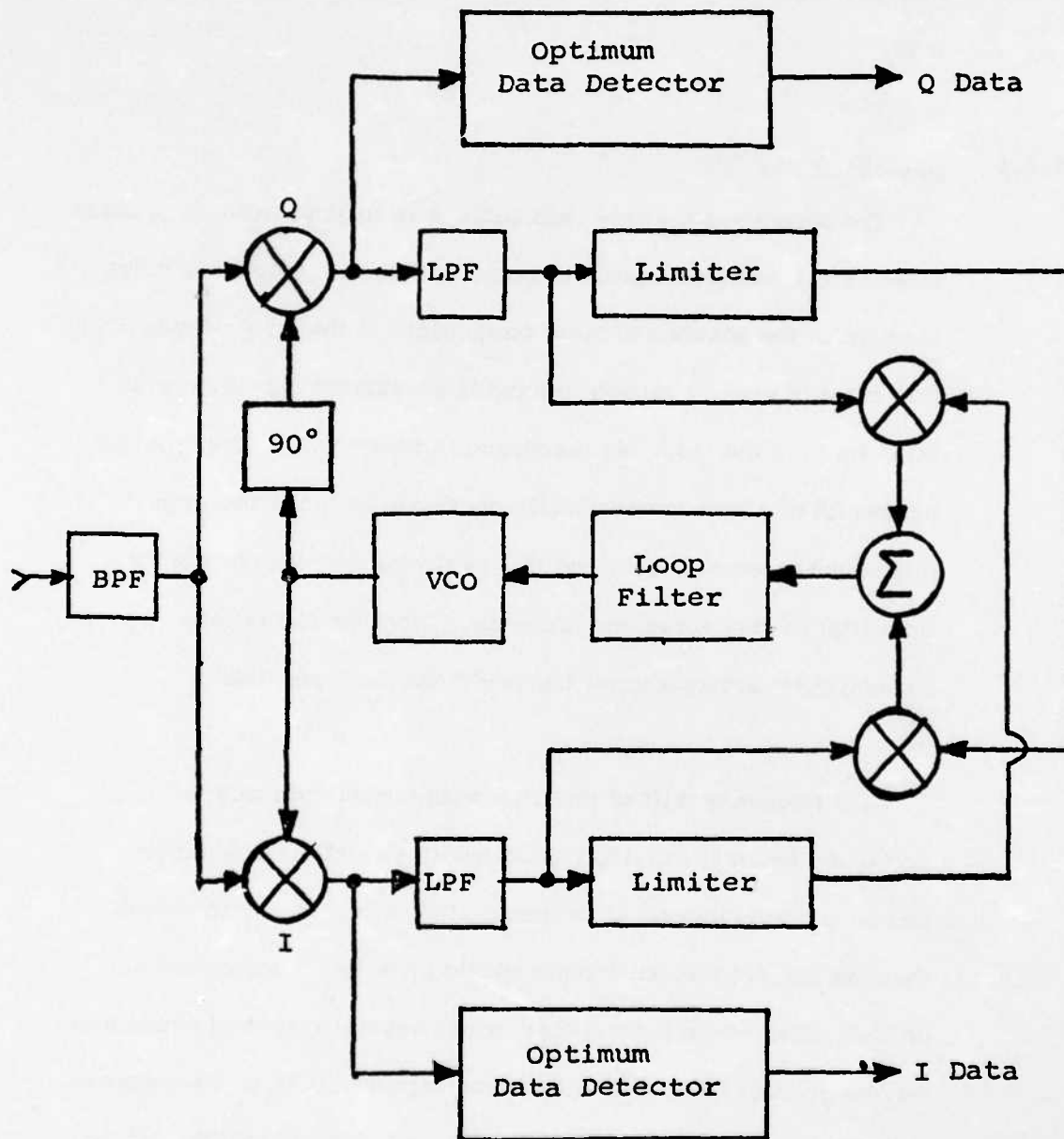


Figure 43. Four Phase Modified Costas Loop

An understanding of each block and its effect upon the overall loop is necessary prior to analysis or design of a modified Costas loop.

#### 2.1.4.2.1 Input Bandpass Filter

The purpose of the bandpass filter is to limit the amount of noise entering the modified Costas loop and thus limit the dynamic range required of the mixers and other components of the loop. If possible, this filter is usually chosen to provide a maximum signal to noise ratio entering the loop. As discussed in section 2.1.2.4 the IF bandwidth of a receiver is usually chosen to be twice the symbol rate of the received signal and this is the optimum bandwidth for this filter in very noisy environments. Other considerations occasionally dictate a wider bandwidth for the input filter.

The frequency drift of the filter with temperature must be accounted for in specifying its bandwidth as well as production and design tolerances. If the transmitter or receiver is in motion then the doppler frequency shift should be added to the bandwidth on both sides of the filter. Also, since several stages of conversion may be employed in a heterodyne receiver as well as in the transmitter, any absolute frequency difference which adds to the relative offset of the signal must be considered as added bandwidth necessary for the filter. These extra considerations for bandwidth are sometimes an order of magnitude greater than the symbol rate. The

mechanization of this filter is dependent upon its center frequency and bandpass characteristics, in conjunction with the stopband requirements for interference rejection. Some forms of realization are tuned cavities, LC circuits, and crystal filters.

#### 2.1.4.2.2 Mixers - I and Q

The purpose of the I and Q mixers is to transfer the center of the modulated carrier to zero hertz so that the data may be recovered and the modified Costas loop derive phase information to correct the VCO. These mixers must have sufficient dynamic range to handle the noise power admitted by the BPF, be capable of operating at the frequency of the carrier, and have DC response at their output. In addition to these characteristics the mixers must be of sufficient bandwidth to handle the data spectrum plus all the other variables mentioned in the previous section. Also since the loop is DC coupled after the mixer outputs, minimum DC offset voltage at the output is desirable. The implementation of the mixers can be any of the devices described in Section 2.1.3.1, and the choice of the type used will be based on the requirements mentioned above.

About the worst case for these mixers occurs when the input filter is much wider than the data rate and allows so much noise through that the signal is completely buried by noise. In this case the total power into the mixer must stay below its maximum operating limit but the signal still must remain above the mixer's lower limit

of DC offset and DC generated by the large noise signal in combination with mixer nonlinearities. This is depicted graphically in Figure 44.

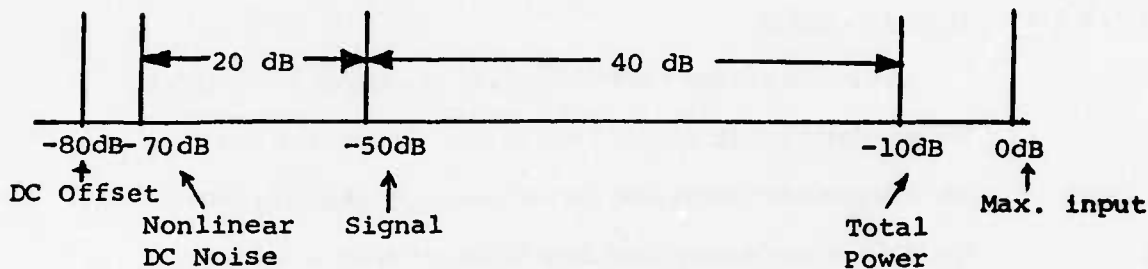


FIGURE 44 Mixer Signal Requirements

Notice that in order to keep the total power into the mixer below the safe maximum the signal is placed very near the lowest operating point of the mixer shown. For this case a mixer with only 50dB of range would be inadequate.

Since the mixer is being used as a phase detector an important quantity is the gain of the mixer. Gain is defined as the ratio of the output voltage change to an input phase change.

$$K_d = \frac{\Delta V_o}{\Delta \phi_i} \quad \text{Volts/Radian} \quad E_Q 12$$

where

$K_d$  = mixer gain

$\Delta V_o$  = Output change in volts

$\Delta \phi_i$  = Input phase change in radians.

The mixer gain will vary with the implementation selected and this is sometimes an important consideration. Too low a mixer gain means that an excessive amount of DC coupled gain must follow the mixers and this is not usually desirable due to the difficulty in realizing large amounts of stable DC gain.

#### 2.1.4.2.3 Low Pass Filters - I and Q

The purpose of the low pass filters in the I and Q channels is to provide optimum filtering for the data signals and thus maximize the signal to noise ratio before the limiters. Since these filters are the low pass equivalents of the input bandpass filter one would make these filters equal to the data rate or less. This especially holds true where the input filter was forced to be much wider than twice the symbol rate and thus admitted a large amount of noise.

The realization of these low pass filters may take one of many different forms, RC, LC, RLC, Butterworth, Chebyshev, and single or multipole. Whichever form is selected the purpose is to maximize SNR. The selection will be based upon the allowed SNR degradation, cutoff frequency, and cost.

For multiple data rate communications one could switch the I and Q LPF's but use the same input BPF for several data rates providing that the dynamic range of the I and Q mixers is not

exceeded. Such an implementation is attractive since the LPF's are usually cheaper than their bandpass equivalent, especially at low data rates. Also, switching the LPF's is usually easier to accomplish than with their bandpass equivalents and the switches themselves are sometimes cheaper. This form of variable data rate loop is therefore particularly attractive.

#### 2.1.4.2.4 Limiters - I and Q

The purpose of the I and Q hard amplitude limiters is to provide an estimate of the symbol polarity for use in the third mixers. Their implementation is usually in the form of analog comparators or open loop amplifiers. The most important parameter of the limiters is that the time delay through them be as small as possible since the data estimate should arrive at the third mixer simultaneously with the filtered analog signal from the other channel. A small amount of hysteresis is sometimes included in the limiters to prevent them from chattering or oscillating.

The usual care must be taken with the I and Q limiters as one would with any high gain, high speed comparator. Circuit layout, stray capacitance, output loading, and offset voltages and currents are potential sources of trouble.

#### 2.1.4.2.5 Third Mixers - I and Q

The purpose of the third mixer is to multiply the filtered analog

output of one channel by the estimated symbol polarity of the opposite channel. The multiplication should occur without delay, or at worst with equal delay from both the limited and the analog input ports. Factors such as speed, bandwidth, and settling time become more important as the data rate increases. The DC offset out of the mixer should be minimized and it should have DC response at all ports. Some possible implementations of third mixers are differential amplifiers, switched or controlled gain amplifiers, and inverting and non-inverting amplifiers followed by switches and a summer. In all cases slew rate of any amplifiers, switching time and DC offsets deserve particular attention.

Sometimes one will encounter the nomenclature "phase detectors" used for third mixers and care should be taken not to confuse this with the I and Q phase detectors (mixers).

#### 2.1.4.2.6 Voltage Controlled Oscillator

The voltage controlled oscillator, or VCO as it is commonly called is one of the most important and expensive components in the modified Costas loop. The center frequency and maximum frequency offset achievable with the control lead are usually the starting parameters one would determine when specifying a VCO. The center frequency is determined by system considerations, usually. For example, the IF frequency may be fixed or the data rate may be too high to operate at a lower IF frequency.

The necessary frequency offset achievable via the tuning lead is composed of several factors, many of which have been considered in Section 2.1.4.2.1 dealing with the input bandpass filter. The tuning range of the VCO should accomodate the total of the following frequency offsets as a minimum:

1. Doppler of the incoming signal
2. LO offsets of RCVR and XMTR
3. Absolute offset of VCO center frequency
4. Drift of VCO center frequency with temperature
5. Drift of VCO center frequency with time
6. Modified Costas loop tuning (dynamic) range.

As mentioned before in relation to the input bandpass filter, the sum of the above items may be several times greater than the symbol rate under consideration and cannot be neglected when specifying the VCO. The mechanization of the VCO is strongly dependent on the ratio of required tuning range to center frequency of operation. Ratios of about .1% are easily achievable with a voltage controlled crystal oscillator or VCXO. Ratios larger than .1% are more readily built using inductors and capacitors (LC) as the frequency determining elements in the oscillator circuits. Such oscillators are generally called voltage controlled oscillators (VCO). The ratio of tuning range to oscillator center frequency is inversely proportional to the Q of the frequency determining elements used in the oscillator.

Besides tuning range and center frequency a third important parameter of a VCO (or VCXO) is the output phase noise. Referring back to Figures 23 and 24 in Section 2.1.1.2 we are reminded of the deleterious effect noise has on the ability of a receiver to correctly estimate the phase of a transmitted signal. In that section we considered the noise as being added to the transmitted signal in its passage through a noisy channel medium, but in this section we are considering the noise as added to the reference carrier estimate. For our purposes of comparing bit error rate performance, or  $E_b/N_0$  degradation, noise added to either the signal or the reference carrier estimate is equivalent. Therefore, the VCO phase noise should be of an acceptable level such that it will not degrade the  $E_b/N_0$  by more than the allowed amount.

For higher data rates such as 10KBPS a large amount of noise enters the loop through the input bandpass filter plus I and Q low pass filters, and thus the VCO noise is usually negligible. For low data rates such as 75 BPS, only a very small amount of noise enters the loop compared to 10 KBPS and now the VCO phase noise may no longer be negligible. Indeed the phase noise of a VCO could be greater than the incoming noise and result in a gross degradation of  $E_b/N_0$  and consequently a poor bit error rate. As a result, the phase noise of a VCO or VCXO is usually specified as a few degrees of peak to peak phase jitter during a bit period or symbol period.

In carrier loop calculations the most needed parameter concerning a VCO is its gain  $K_O$ , defined as the ratio of an output frequency change to an input voltage change.

$$K_O = \frac{\Delta W_O}{\Delta V_I} \frac{\text{Radians/Sec}}{\text{Volt}} \quad \text{EQ.13}$$

Where  $K_O$  = VCO gain

$\Delta W_O$  = Output frequency change in radians per second

$\Delta V_I$  = Input voltage change in volts

Notice that the units associated with the VCO gain are such that the product  $K_O K_d$  has the units of inverse time, i.e. frequency. This product  $K_O K_d$  is called loop gain,  $K_v$ , and will be encountered in most loop equations.

#### 2.1.4.2.7 Phase Shifter - 90°

The 90° phase shifter is used to provide two local oscillators of the same frequency but in quadrature phase for mixing the modulated carrier down to zero frequency. The most significant parameter of the 90° phase shifter is the accuracy with which it achieves 90° of phase shift. If the phase difference is not exactly 90° then some of the I channel signal will appear in Q channel and some of the Q channel signal will appear in the I channel. If we define the amount of phase shift provided as 90° +  $\Theta_e$ , where  $\Theta_e$  is the amount of phase error in the 90° phase shifter, then the amount of undesired signal in the desired channel is obtained as follows:

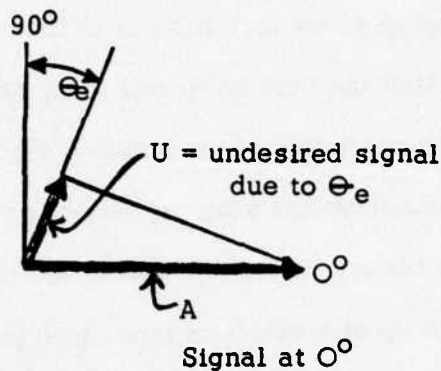


Figure 45. Undesired Signal Due to  $\Theta_e$

Figure 45 shows a signal of amplitude  $A$  lying at  $0^\circ$  and a phase shift angle of  $90^\circ + \Theta_e$  where  $\Theta_e$  is a small negative number. The interference  $U$  is seen to be the projection of signal  $A$  upon  $90^\circ + \Theta_e$  and the magnitude of this projection is given by:

$$|U| = |A \sin(\Theta_e)| \quad \text{EQ. 14}$$

The magnitude of the phase error usually allowed is on the order of a few degrees.

Several different mechanizations of the  $90^\circ$  phase shifter are possible depending upon the frequency range and accuracy desired. Low frequencies in the audio region would allow RC shifters to be used, medium RF frequencies make LC shifters and hybrids more practical. The RF hybrids actually serve a dual purpose in that they split the LO signal to the I and Q channels as well as providing  $90^\circ$  of phase shift.

#### 2.1.4.2.8 Loop Filter

The purpose of the loop filter is to filter noise from the phase information after the third mixer and to shape the overall frequency response characteristics of the modified Costas carrier loop. The loop filter will determine such parameters as loop bandwidth, loop gain, and damping factor. These parameters will in turn affect the loop SNR, the lock up or acquisition time, loop phase error, and the maximum allowed doppler rate. These parameters are very significant and are determined by the performance requirements of the modified Costas Loop. The loop filter must be designed with the appropriate characteristics and parameters to provide proper loop performance.

The majority of modified Costas loops employ second order loop filters, either passive or active. The equations relating Costas loop performance to loop filter parameters are slightly different according to the use of passive or active loop filters. This section will deal only with these second order loop filters but will discuss the differences between the passive and active implementations. An excellent reference on loop analysis and design is "Phaselock Techniques" by Floyd M. Gardner should the reader desire a more in-depth treatment of phaselocked loop performance.<sup>3</sup>

Figure 46 is a basic loop block diagram and shows the quantities necessary for the derivation of the elementary loop equations

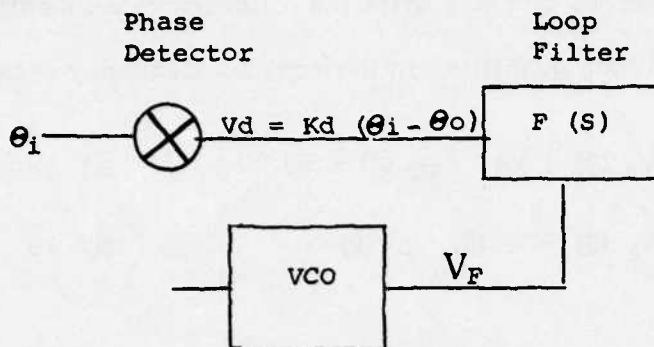


Figure 46. Basic Loop, Block Diagram

In section 2.1.4.2.6 we related VCO output frequency versus input voltage by EQ 13. Rearranging that equation we obtain

$$\omega_o = K_o V_F \quad \text{EQ 14}$$

and recalling that frequency is the derivative of phase.

$$\omega_o = \frac{d\theta_o}{dt} = K_o V_F \quad \text{EQ 15}$$

$$\theta_o(t) = K_o \int V_F dt \quad \text{EQ 16}$$

Notice that the VCO output phase is proportional to the integral of the input voltage in the time domain. Expressing EQ 16 in the complex frequency domain by means of Laplace transforms leads to EQ 17.

$$\theta_o(s) = \frac{K_o V_F(s)}{s} \quad \text{EQ 17}$$

Referring to Figure 46 one may write the following relationships between certain loop quantities in the complex frequency domain.

$$V_d (S) = K_d ( \Theta_1 (S) - \Theta_o (S) ) \quad \text{EQ 18}$$

$$V_F (S) = F (S) V_d (S) \quad \text{EQ 19}$$

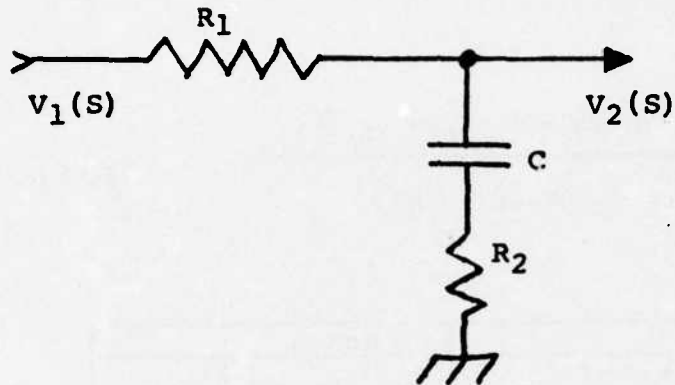
The basic loop equations may then be derived from equations 17, 18, and 19.

$$\frac{\Theta_o (S)}{\Theta_1 (S)} = H(S) = \frac{K_o K_d F (S)}{S + K_o K_d F (S)} \quad \text{EQ 20}$$

$$\frac{\Theta_1 (S) - \Theta_o (S)}{\Theta_1 (S)} = \frac{\Theta_e (S)}{\Theta_1 (S)} = \frac{S}{S + K_o K_d F (S)} \quad \text{EQ 21}$$

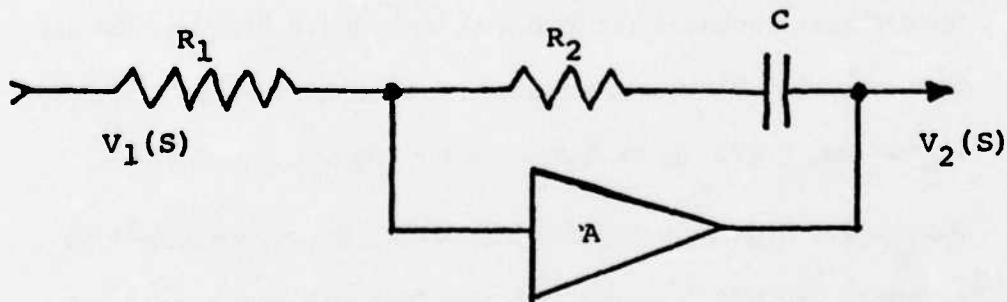
Equation 20 relates VCO output phase to signal input phase and is commonly called the transfer function of the loop. Equation 21 describes the ratio of phase error between the input signal phase and VCO output phase as a function of frequency.

The next logical extension of the transfer function equation is the inclusion of the exact function or description of  $F (S)$ . At this point the difference between active and passive second order loop filters must be analyzed. Figure 47 shows both types of filters and their transfer functions. Upon substituting these functions into equation 20 one obtains the transfer functions for both active ( $H_A (S)$ ) and passive ( $H_P (S)$ ) loops.

PASSIVE LOOP FILTER

$$F_P(s) = \frac{V_2(s)}{V_1(s)} = \frac{s\tau_2 + 1}{s(\tau_1 + \tau_2) + 1}$$

$$\tau_1 = R_1 C \quad \tau_2 = R_2 C$$

ACTIVE LOOP FILTER

$$F_A(s) = \frac{s\tau_2 + 1}{s\tau_1} \quad \text{for large } A$$

$$\tau_1 = R_1 C \quad \tau_2 = R_2 C$$

Figure 47. Passive and Active Loop Filters

$$H_A(S) = \frac{2z W_n S + W_n^2}{S^2 + 2z W_n S + W_n^2} \quad \text{EQ 22}$$

$$H_P(S) = \frac{S W_n (2z - W_n/K_O K_d) + W_n^2}{S^2 + 2z W_n S + W_n^2} \quad \text{EQ 23}$$

Where:

Passive	Active
$W_n = \left( \frac{K_O K_d}{\tau_1 + \tau_2} \right)^{\frac{1}{2}}$	$W_n = \frac{K_O K_d}{\tau_1}^{\frac{1}{2}}$
$z = \frac{1}{2} \left( \frac{K_O K_d}{\tau_1 + \tau_2} \right)^{\frac{1}{2}} \left( \tau_2 + \frac{1}{K_O K_d} \right)$	$z = \frac{\tau_2}{2} \left( \frac{K_O K_d}{\tau_1} \right)^{\frac{1}{2}}$

Common terminology for these quantities is "natural frequency of the loop" for  $W_n$  and "loop damping factor" for  $z$ . Notice that the difference between the loop with the passive filter and the one with the active filter depends on the ratio of loop natural frequency  $W_n$  to "loop gain"  $K_v = K_O K_d$ . When  $W_n/K_O K_d \ll 2z$  the passive filter loop equation approaches the active filter loop equation, and this is usually the case in a high gain second order loop, the type we are concerned with here.

Inspection of equations 22 and 23 reveals that both transfer functions are those of a low pass filter. The loop will pass low frequency changes ( $\ll W_n$ ) without attenuation but the frequency

response rolls off 6 dB per octave beginning near  $W_n$  so that high frequency components present at the signal input are attenuated at the VCO output. This low pass function acts as a bandpass function for noise ( $BW \approx W_n$ ) centered about the input carrier frequency and serves to increase the signal to noise ratio of the derived carrier reference by effectively narrowing the bandwidth since the IF bandwidth is usually much wider than  $W_n$ . The resultant output signal to noise ratio is approximated by equation 24.

$$SNR_O = \frac{B_{IF}}{W_n} SNR_{IF} \quad \text{EQ. 24}$$

Where:

$SNR_O$  = VCO output SNR

$SNR_{IF}$  = IF SNR in  $B_{IF}$

$B_{IF}$  = IF noise BW

Typical loop design dictates a minimum VCO output signal to noise ratio of 20 dB to 40 dB for most Costas loop demodulators. The high loop SNR is required in order for the modified Costas loop to provide the receiver with an accurate estimate of the input carrier reference phase to be used in data detection. Since data is not expected to be correctly detected until the loop is actually in "lock" or tracking the input phase, a common practice is to widen the loop bandwidth for initial acquisition and then switch to a narrower loop bandwidth when in lock to provide a better carrier estimate.

Continuing our assumption about the high gain second order loop, we write the phase error of the loop versus frequency as Eq 25.

$$\frac{\Theta_e (S)}{\Theta_i (S)} = 1 - HA (S) = \frac{S^2}{S^2 + 2z W_n S + W_n^2} \quad \text{EQ 25}$$

Note that equation 24 describes zero phase error ratio at  $S = 0$  and a phase error ratio equal to 1 at  $S = \infty$ . This implies that the loop will track or follow the input signal for slow phase changes ( $< W_n$ ) but ignores high frequency changes ( $> W_n$ ), just as we deduced from the transfer function equation.

The most useful phase error quantity is the static phase error arising from a frequency offset between the incoming signal and the nominal center frequency of the VCO. This frequency offset may be caused by doppler offset due to relative motion of the transmitter and receiver or by a relative offset of their frequency standards. If we define the total frequency offset as  $\Delta w$  then the static phase error  $\Theta_v$  is given by equation 26.

$$\Theta_v = \frac{\Delta w}{K_v} \quad \text{EQ 26}$$

Where  $K_v = K_o K_d F(0)$

which is

$K_v = K_o K_d$  passive loop filter

$K_v = K_o K_d A$  Active loop filter

The static phase error can be made arbitrarily small by increasing  $K_v$  according to equation 26. This is especially easy in the case of an active loop filter since  $K_v$  is proportional to  $A$ , the amplifier open loop gain. Modern operational amplifiers make small static phase errors achievable when necessary for demodulator performance.

The equations in this section may be used to determine the loop filter parameters once the overall demodulator performance is defined. However, a method which is sometimes easier than direct numerical calculation is graphical analysis. The accuracy of graphical methods is less than the numerical calculations but it is often accurate enough for initial estimates and even final designs. An example of the determination of a second order loop filter will be presented.

Referring to equation 26 one determines loop gain  $K_v$  by specifying frequency offset  $\Delta\omega$  and static phase error  $\Theta_v$ . For 1KHz frequency offset and  $3.6^\circ$  tracking error,

$$\begin{aligned}\Delta\omega &= 2\pi \times 1000 \text{ Rad/Sec} \\ \Theta_v &= 2\pi \times 3.6^\circ/360^\circ \\ K_v &= \frac{\Delta\omega}{\Theta_v} = 100,000 = 100 \text{ dB}\end{aligned}$$

This value of  $K_v$  is plotted at  $\omega = 1 \text{ rad/Sec}$  on the graph in Figure 48 and a line with a slope of 6dB/octave or 20 dB/decade is drawn through the point. This corresponds to the VCO which is an integrator and thus has a single pole at  $S = 0$ .

Next from equation 24 the required loop bandwidth  $w_n$  is determined by specifying IF SNR, loop SNR, and IF BW. For an IF BW of 20 KHz, IF SNR of 0dB and loop SNR of 26dB we have,

$$B_{IF} = 2\pi \times 20,000 \text{ Rad/Sec}$$

$$SNR_{IF} = 0\text{dB} = 1$$

$$SNR_L = 26\text{dB} = 200$$

$$W_n = \frac{SNR_{IF}}{SNR_L} B_{IF} = 2\pi \times 100 = 628 \text{ Rad/Sec.}$$

This value of  $W_n$  is plotted on the 0dB gain axis and a line with a slope of 12dB/octave or 40dB/decade is drawn through it. The intersection of this line with the 6dB/octave line drawn through  $K_v$  defines the radian frequency of the first breakpoint in the loop filter which is equal to  $1/\tau_1$ .

Finally, a line with a slope of 6dB/octave is drawn through a point on the  $W_n$  line corresponding to 6 dB loop gain for  $z \approx .707$  or through the 10dB point for  $z \approx 1.0$ . The intersection of this line with the  $W_n$  line at the 6dB or 10dB point defines the radian frequency of the second breakpoint in the loop filter, equal to  $1/\tau_2$ . At this point  $K_v$ ,  $\tau_1$ ,  $\tau_2$ , and  $z$  are all known and the open loop response has been plotted. The closed loop response will follow the equations presented in this section.

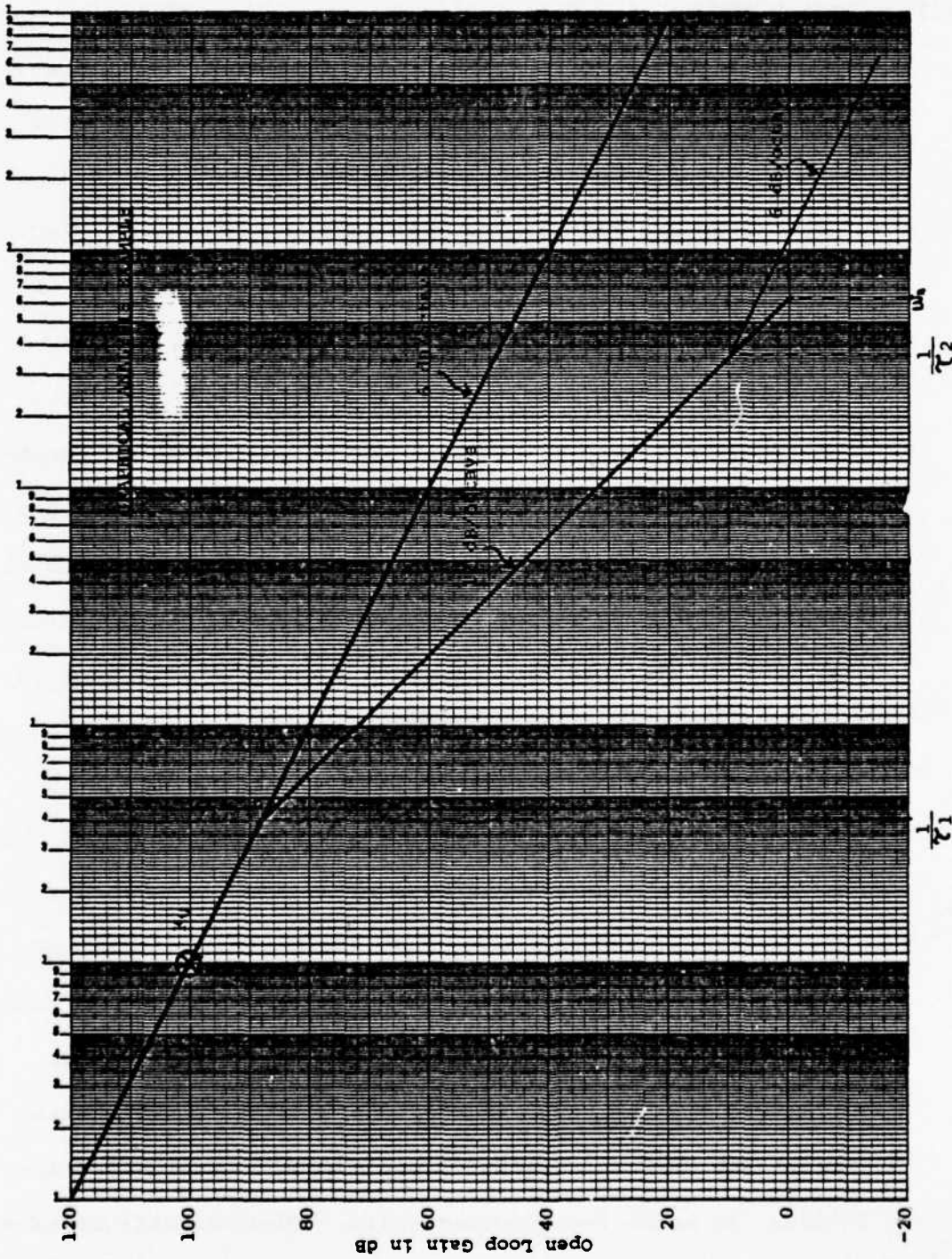


Figure 48. Graphical Analysis Example

## 2.1.5 Implementation of Bit Timing Loop

### 2.1.5.1 Block Diagram and Description

The purpose of the bit timing loop is to extract a bit timing clock from the incoming data modulation. Bit timing information is needed when implementing optimum data detectors and is also used to clock the demodulated data into equipment following the Costas demodulator. A generalized block diagram of a bit timing loop and its connection to the modified Costas carrier loop are shown in Figure 49. The reader will notice that with the exception of a transition detector the bit timing loop is identical to the phase locked loop of Figure 46 in the section dealing with loop filters and loop analysis. This similarity means that all the loop equations derived in that section are applicable to the bit timing loop, and as a result, only the mechanistic differences will be treated here.

The general requirements of a bit timing loop are that it provide a stable squarewave clock that is synchronized to the incoming data, have minimum static phase error or "timing error", and possess only a small amount of FM noise or clock "edge jitter". Synchronization to the data is achieved via the phase locked loop, and the static phase error and FM noise are functions of the loop gain and loop signal to noise ratio respectively. These quantities have

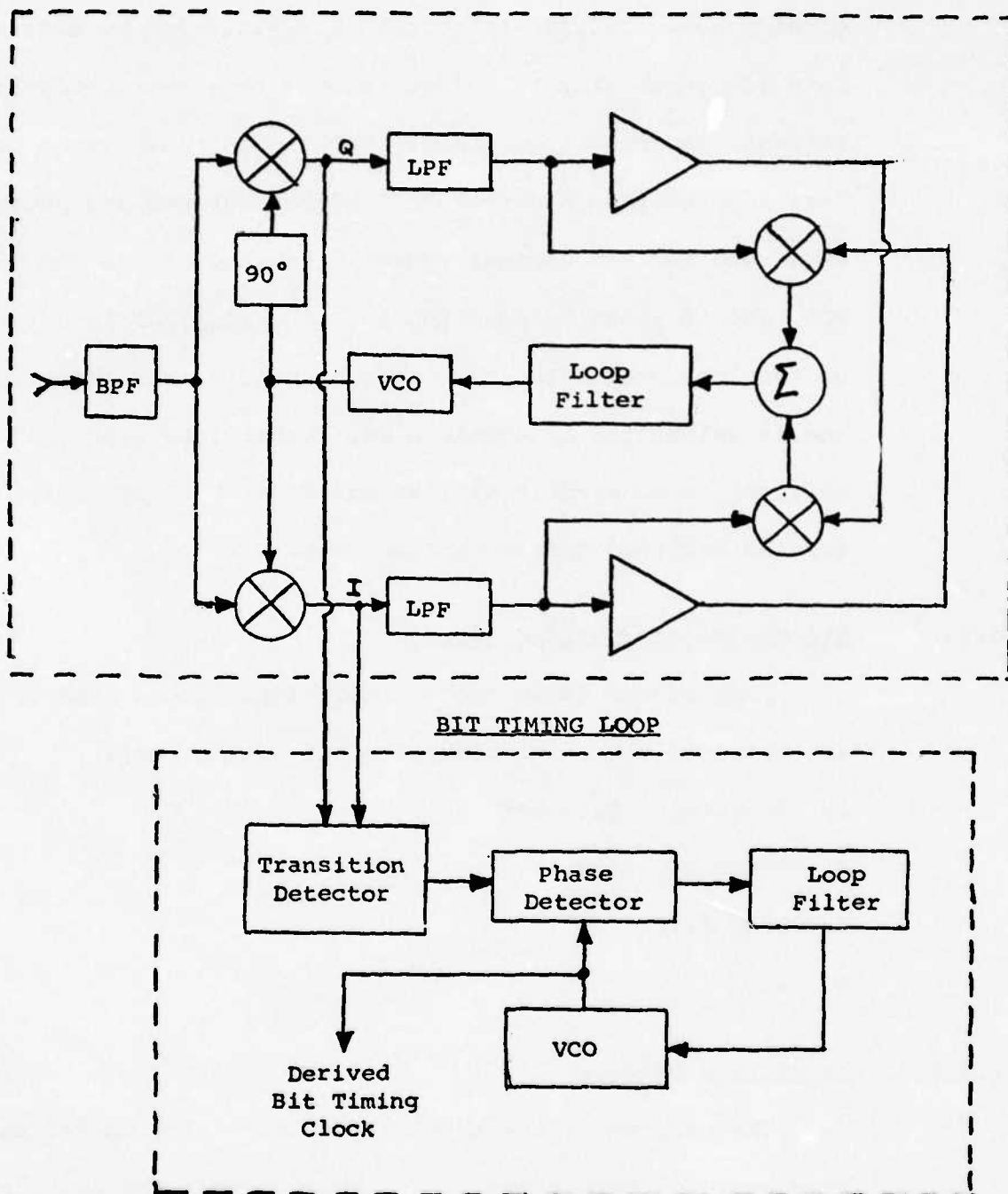
MODIFIED COSTAS CARRIER LOOP

Figure 49. Modified Costas Carrier Loop and Bit Timing Loop

already been analyzed in section 2.1.4.2.8 and we already have the capability to calculate them once the appropriate external factors are defined. The static phase error calculation involves the frequency offset between the incoming data rate and the nominal center frequency of the bit timing VCO, and is given by equation 26. The loop SNR is a function of the loop bandwidth, the input bandwidth, and input SNR, and is calculated by equation 24. Other loop quantities are obtained in an exactly similar manner to that determined for the modified Costas carrier loop.

#### 2.1.5.2 Discussion of Specific Blocks

From Figure 49 we can identify four blocks that are essential to the operation of a bit timing loop:

1. Transition Detector
2. Phase Detector
3. Loop Filter
4. VCO

##### 2.1.5.2.1 Transition Detector

The purpose of the transition detector is to define the time at which data transitions occur so that the bit timing phase locked loop can adjust the phase of the VCO to align the clock edges with the data edges. The transition detector usually consists of limiters and inverters followed by RC coupled AND gates. The limiters may be the I and Q limiters

contained within the Costas loop, or external limiting may be employed in the transition detector. The inverters are necessary to define both positive and negative transitions, and the RC coupled AND gate acts as a one shot which supplies a single narrow pulse for every transition.

Note that in Figure 49 both I and Q channels are shown as connected to the transition detector. This is necessary for QPSK and SQPSK since data is present in both channels and thus transition information can be derived from both. In BPSK, however, only the I channel has data present and so only one input to the transition detector is needed.

#### 2.1.5.2.2 Phase Detector

The purpose of the bit timing phase detector is to measure the phase difference between the clock edges and the data edges or transitions. A common method for doing this is shown in Figure 50. Here the bit timing clock is used to generate a ramp and the output of the transition detector is used to sample this ramp and charge a capacitor at the loop filter input. This type of phase detector has nearly a  $360^\circ$  or  $2\pi$  lock range and is popular for many applications. Its gain is very accurately determined as  $K_D = V/2\pi$  volts/radian and this phase detector can be quickly modified to maintain constant gain for variable bit rates.

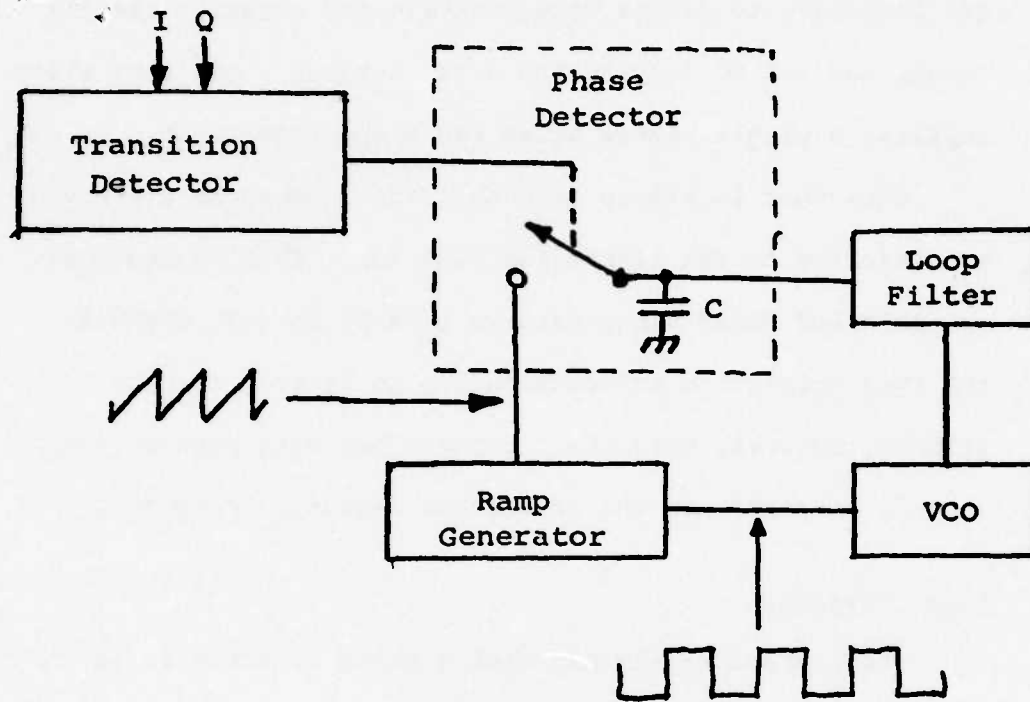
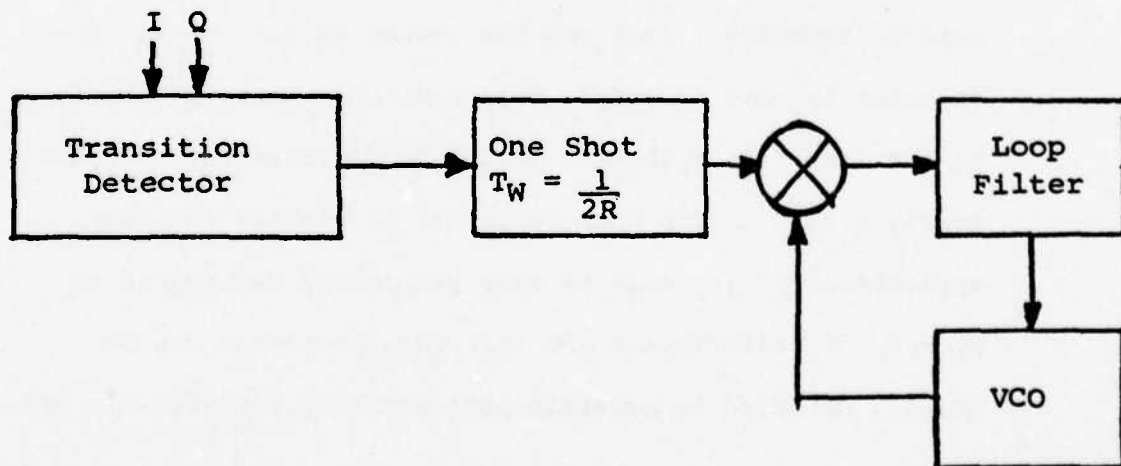
RAMP/SAMPLE/HOLD BIT TIMING LOOPONE SHOT BIT TIMING LOOP

Figure 50. Bit Timing Phase Detector

A second type of phase detector is also shown in Figure 50 and this employs a one shot with  $T_W = \frac{1}{2R}$  plus a regular mixer or multiplier. The one shot pulse width is such that if it is hit with a transition indication every  $T = 1/R$  seconds then it will put out a squarewave with a period of  $T$  seconds or at a rate  $2R$ . This is the same frequency and phase as the bit timing clock should be but it is very noisy so the phase locked loop is used to remove the noise and fill in squarewaves where there are no data transitions. The mixer used in this loop can be the same implementation type as the third mixers in the Costas loop, or it may be a mixer suited to only squarewave inputs such as a digital exclusive OR gate. The digital exclusive OR gates have a phase detector gain which is given by  $K_D = (V_{HIGH} - V_{LOW})/\pi$  volts/radian and requires much filtering to remove the strong squarewave components.

#### 2.1.5.2.3 Loop Filter

The bit timing loop filter is usually chosen to have an  $\omega_n$  between one-tenth and one-hundredth of the data rate depending upon how noisy the signal is and how fast the bit timing loop is required to lock up to the data transition. The latter is usually not a significant consideration since the carrier loop lockup time is normally an order of magnitude larger than the bit timing lockup time.

All of the comments and calculations involving loop equations and loop filters in section 2.1.4.2.8 can be applied to the bit timing loop filter and the reader is referred to that section for loop filter determination.

#### 2.1.5.2.4 Voltage Controlled Oscillator

The VCO for the bit timing loop is exactly analogous to the VCO for the carrier loop and all the comments of section 2.1.4.2.6 apply here also. The only difference between the two oscillators is the center frequency of operation which sometimes allows the bit timing VCO implementation to be of the RC type. This particular implementation is attractive when possible to use it since the entire VCO can be obtained in a single integrated circuit.

#### 2.1.6 Implementation of Data Detection

##### 2.1.6.1 Block Diagram and Description

All methods of data detection involve the periodic sampling at the data rate of some form of averager as shown in Figure 51. The various averagers have had their performance characterized in section 2.1.3.3 on data detection and only their implementation will be considered here.

##### 2.1.6.2.1 Optimum Data Detector

The optimum data detector is a true integrator which integrates the I or Q signal for one bit period. The

practical analog implementation of this data detector requires that it be sampled at the end of the bit period and then the integrator reset to zero for the integration of the next bit period. Figure 51 shows a typical analog implementation of the integrate and dump type of data detector. An operational amplifier is connected as an integrator with the addition of a FET across the integrating capacitor to discharge the integrating capacitor to zero volts at the end of a bit period. Following the integrator is a comparator which provides a continuous estimation of the integrator symbol polarity and thus the data. The D flip-flop is used as a sample and hold of the data estimate from the integrator and this is updated at the bit rate by use of the bit timing clock. The pulse width of the one shot driving the FET is usually set to about  $1/30$  of the bit period so as to contribute a negligible amount of degradation.

#### 2.1.6.2.2 Non Optimum Data Detector

All other data detectors using lowpass filters are non-optimum since they do not provide a true average over one bit period. Figure 52 shows such a non-optimum data detector. It consists of a lowpass filter followed by a limiter and flip-flop. Notice that there is no dumping of the filter so intersymbol interference can occur since some energy will be left in the lowpass filter from previous bits. This degrades the bit error rate in addition to the non-optimum averaging

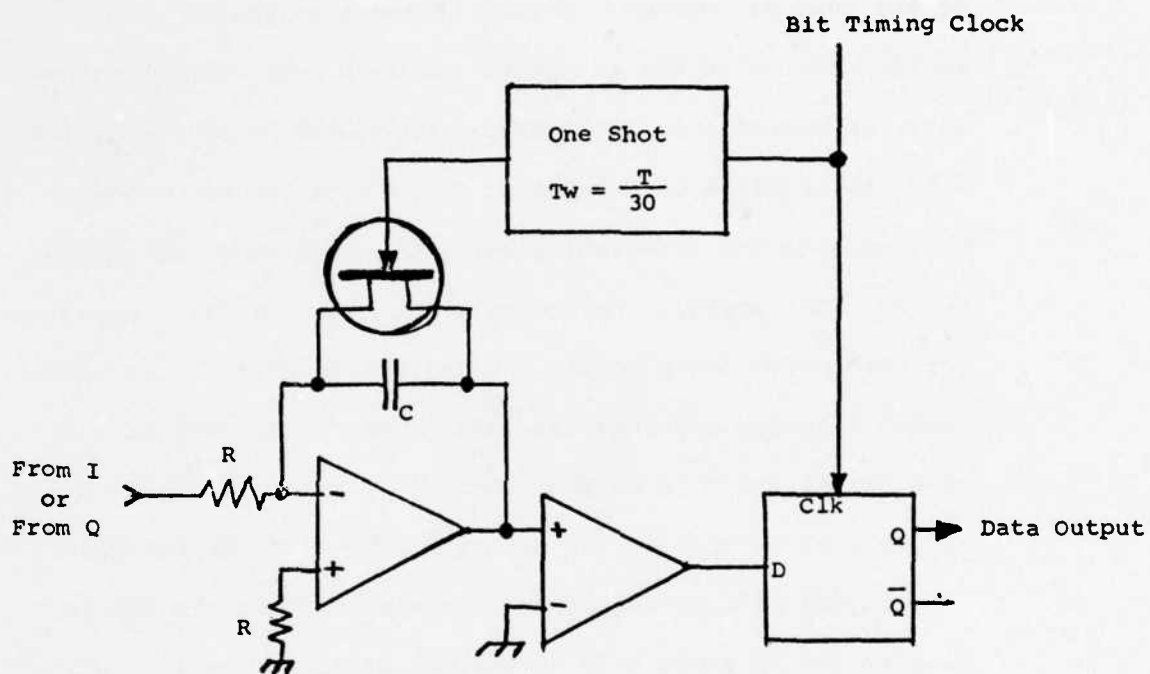


Figure 51. Optimum Data Detector

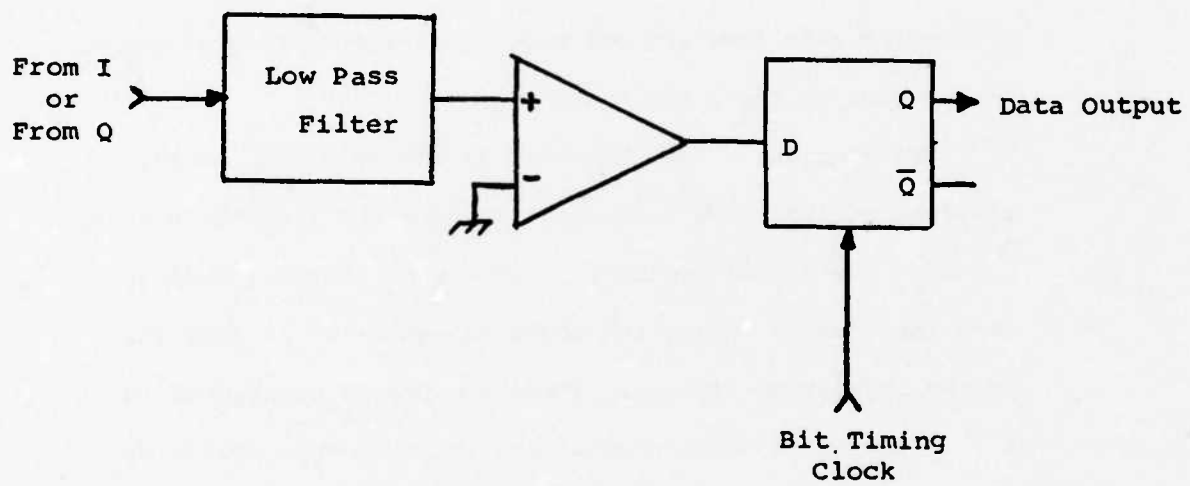


Figure 52. Non-Optimum Data Detector

degradation, but the implementation of the lowpass filter is simpler than the integrator with the discharge FET.

#### 2.1.7 Additional Functions Available

##### 2.1.7.1 Carrier Acquisition Indication

Some form of indicator is usually required in a Costas demodulator to signal the user when the phase locked carrier loop has acquired synchronization with an incoming signal. Many different schemes have been proposed and implemented to accomplish this function but most involve some form of power measurement in the I and Q channels.

The simplest scheme is shown in Figure 53 and merely consists of full wave rectifiers in both the I and Q channels. For BPSK the signal vector will always be in the I channel when the loop is locked but could be either  $0^\circ$  or  $180^\circ$  due to the modulation present. These two phases correspond to a  $\pm 1$  V output in the I channel and the full wave rectifier (FWR) will convert the random output to +1 V. Only noise with zero mean is present in the Q channel, however, and this, when rectified, results in a very small positive voltage which approaches zero volts as the SNR increases. The two FWR outputs are then differenced and lowpass filtered before a comparison is made with a set threshold. This circuit will only indicate acquisition when the signal vector lies in I channel and the component in Q channel is approaching zero.

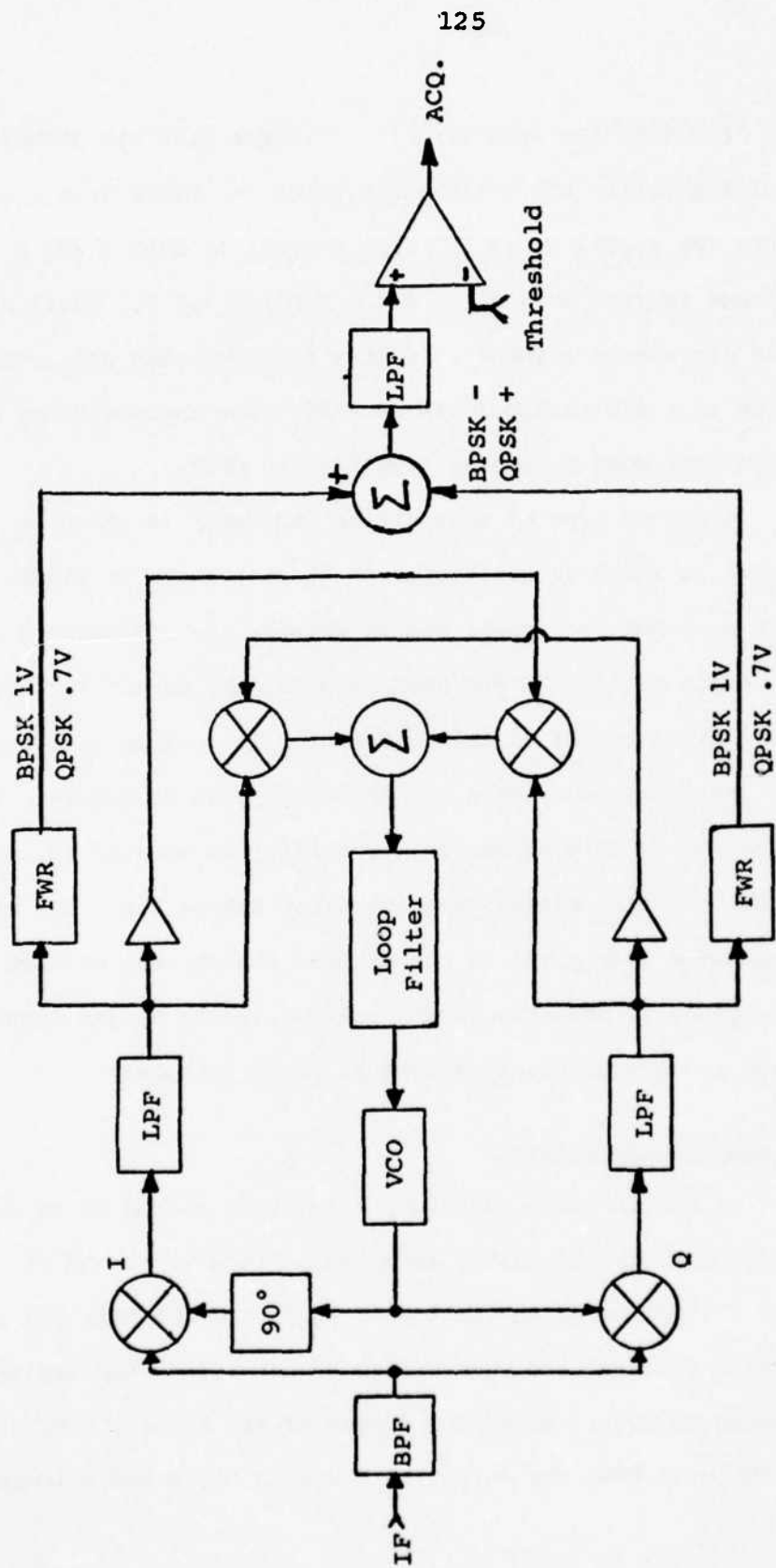


Figure 53. Carrier Acquisition Indication

For QPSK the same circuit is usable with one slight modification to the differencer which is turned into a summer. Since the signal is at  $45^\circ$  with respect to both I and Q the voltage in each channel is  $\pm \sin(45^\circ) = \pm 0.7$  V. These signals are summed together, lowpass filtered, and again compared to a set threshold as in BPSK. The threshold may require adjustment when switching from BPSK to QPSK.

A second type of acquisition indicator is shown in Figure 54 which is quite similar to that shown in Figure 53. Here a window comparator senses whether the differenced output is within  $\Delta V$  of +1 V for BPSK or within  $\Delta V$  of +0.7 V for QPSK. The digital output of this comparator is lowpass filtered and then compared with a set threshold just as before. The advantage of this scheme is its ability to operate at lower signal to noise ratios than the first scheme since the window comparator only gives an output when the channel voltage is very close to what the signal voltage should be and ignores large amounts of noise present at other voltages.

#### 2.1.7.2 Automatic Gain Control

If AGC is required a very convenient method is to use almost the same circuitry as shown in Figures 53 and 54. The summation point of the full wave rectified channels can be lowpass filtered and conditioned to control an AGC amplifier located in the IF or baseband path of the signal. This type of AGC will keep the amount of power in the I and Q lowpass

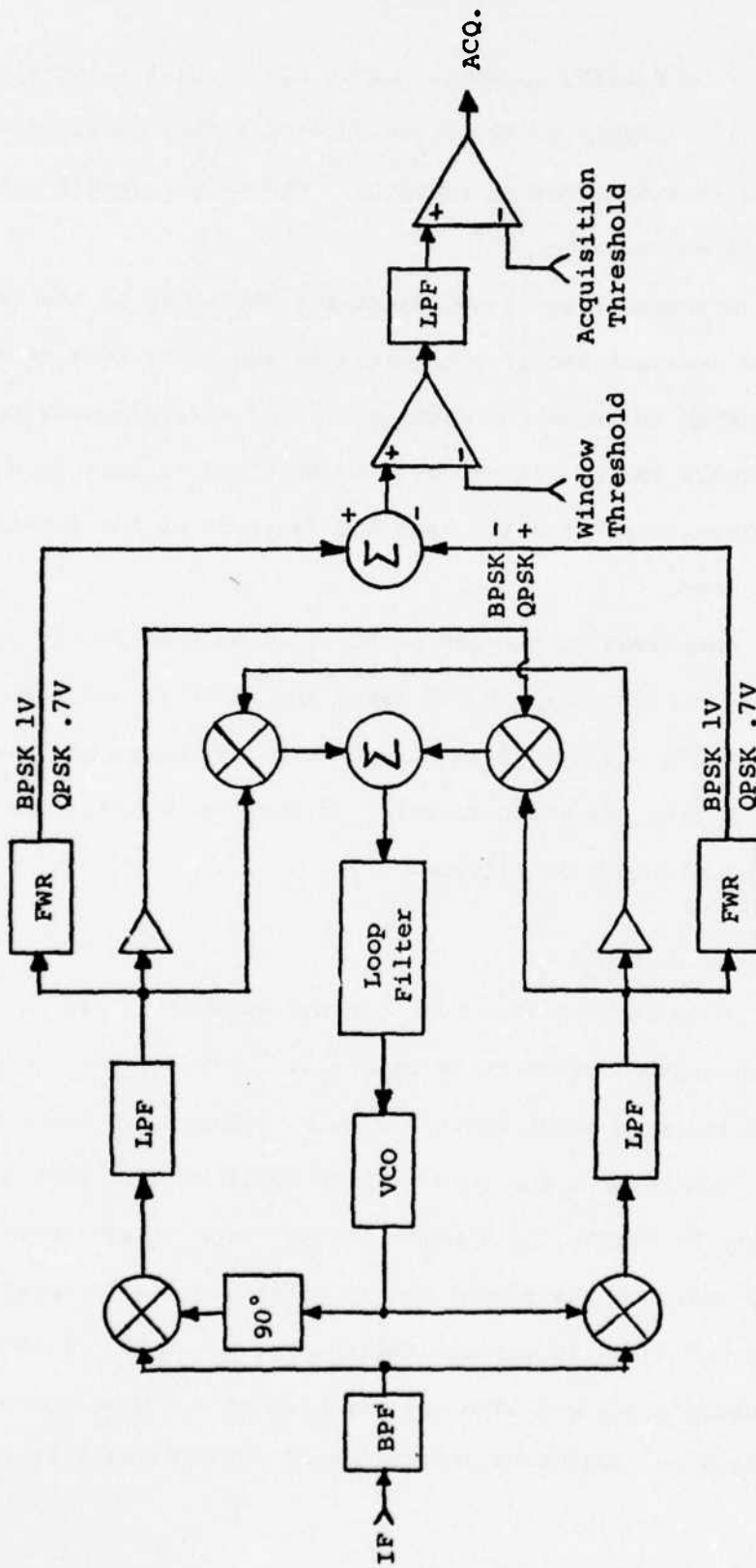


Figure 54. Carrier Acquisition Indication with Comparator

filter bandwidth constant. Since the lowpass filters' cut-offs are roughly equal to the data rate this means constant power in a data rate bandwidth, a convenient result for the Costas demodulator.

A second type of AGC maintains the power in the IF bandwidth constant and is equivalent to the first type of AGC if the IF BW is twice the data rate. For multiple data rate receivers the IF filters must be switched in this type of receiver to provide the same AGC function as the first scheme mentioned.

Sometimes both types of AGC will be used in the same receiver. The main IF AGC keeps the first IF amplifiers from being overloaded and the baseband IF keeps the power in a data rate bandwidth constant so that demodulation and carrier acquisition are simplified.

#### 2.1.7.3 FSK and FM Audio

A modified Costas loop has the capability for detecting FM modulation since it is basically a phase locked loop that will track an input carrier with or without PSK modulation. The requirements for this type of operation are that the signal be within the dynamic tuning range of the phase locked loop and that the signal change frequency slowly enough so the loop can track it without falling out of lock. If these conditions are met then one may observe the VCO control line voltage and obtain an indication of what the carrier frequency

is with respect to time. A phase locked FM demodulator is the overall result and the performance of this class of FM detector has been analyzed and documented in the literature.

The rough rules governing this type of detector are easily visualized by recalling that the transfer function  $H(s)$  of a phase locked loop is a lowpass filter. This can be transformed into a bandpass function about the carrier also. This implies that any frequency component desired to be detected should be less than the cutoff frequency of the loop, or approximately  $\omega_n$ . The second limitation is imposed by the fact that the loop cannot track frequencies outside its tuning range, and thus the signal is constrained to lie within this range.

The final result of these observations is that in order to make an FM detector one must construct the loop with adequate dynamic tuning range and modify  $\omega_n$  of the loop to include the highest frequency of interest. The VCO control lead can then be conditioned by buffering for FM audio detection or hard decisions made for FSK detection.

2.2. SPECIFIC CASE2.2.1 Demodulator Specifications

<u>Item</u>	<u>Requirement</u>
Modulation Format	SQPSK
Data Rate 1	10 KBPS
Data Rate 2	100 KBPS
IF Frequency	70 MHz

2.2.2 Implementation of Demodulator2.2.2.1 Block Diagram and Description

The overall block diagram of an SQPSK Costas demodulator is shown in Figure 55. The signal flow from the 70 MHz IF input to the digital data output is as follows. A 70 MHz SQPSK modulated signal is applied to the input of a 70 MHz preamp which provides low noise gain and reverse isolation. This amplifier is also capable of automatic gain control action, or AGC, via a DC voltage control line. The power in the front end bandwidth is thus kept constant by the 70 MHz AGC amplifier. The AGC leveled 70 MHz signal is then downconverted in a mixer by a 59.3 MHz crystal oscillator to the second IF frequency of 10.7 MHz. Next, the signal is band limited by a crystal filter with a bandwidth of approximately twice the symbol rate, which for SQPSK modulation is equal to the data rate. These IF filters are switchable for either 10 KBPS or 100 KBPS operation. A 10.7 MHz limiting amplifier follows

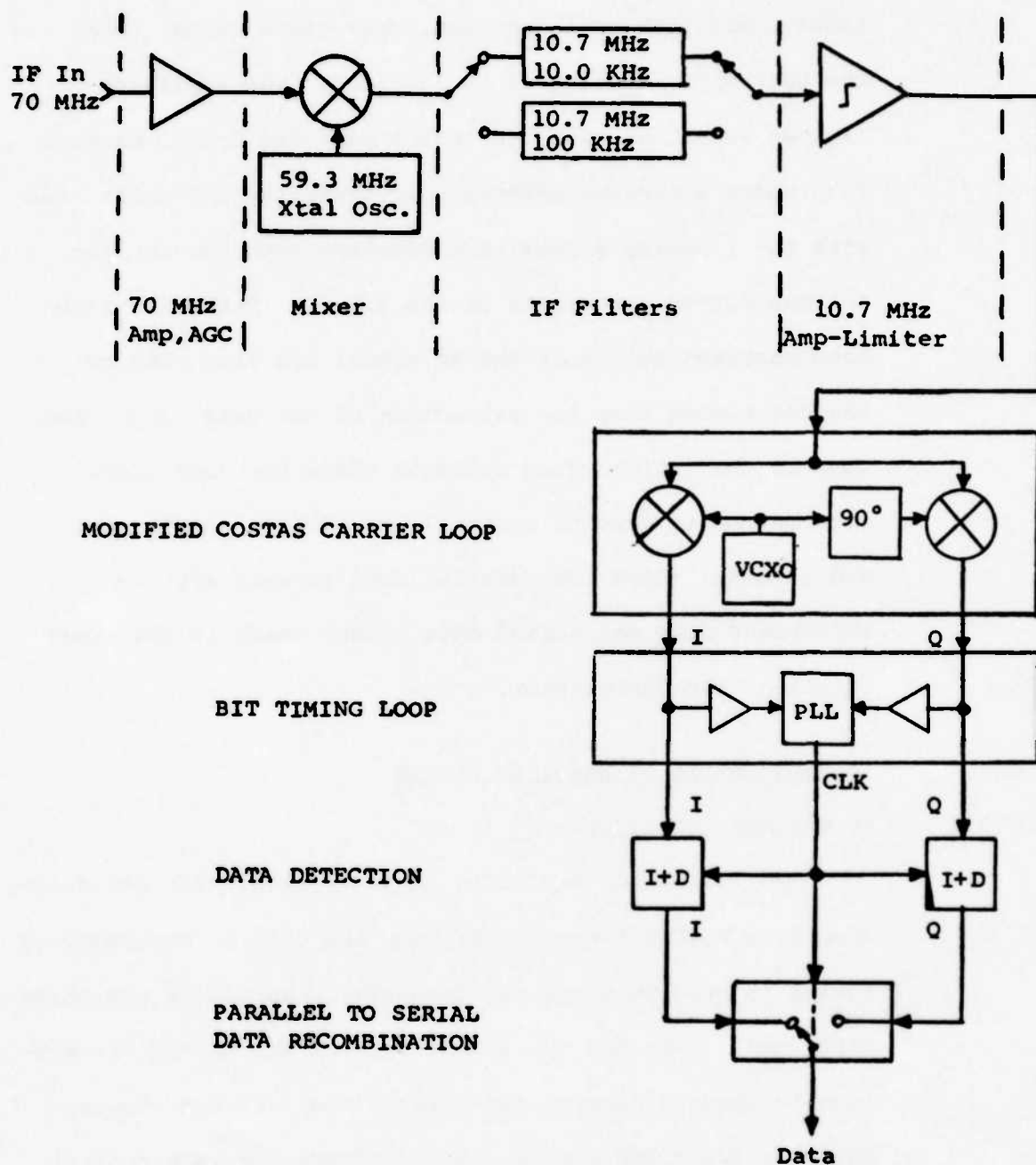


Figure 55. Demodulator, Block Diagram

the IF filters and produces a constant power in the IF filter bandwidth on an instantaneous basis rather than the very slow leveling of an AGC loop. The amplitude limited signal is then fed to the modified Costas carrier loop where a carrier reference is extracted and multiplied with the incoming signal thus deriving both the inphase and quadrature components of the signal. These two base-band representations of the RF signal are then sent to the bit timing loop for extraction of the data clock, and then to the optimum data detector where the data clock information is used to optimally decode the resultant I and Q data. These two parallel data streams are then recombined into one serial data stream which is the final output of the demodulator.

### 2.2.3 Implementation of Specific Blocks

#### 2.2.3.1 70 MHz AGC Amplifier

The 70 MHz AGC amplifier is implemented with low noise, dual gate MOSFET transistors, type RCA 40822. Broadband LC tuning is used to shape the frequency response of the three stage amplifiers and the second gate of the MOSFET transistors is used to control the gain of the last two stages, thus providing AGC action. A DC voltage for gain control is derived from the output of the last stage with a diode rectifier. This voltage is then amplified, low pass filtered, and level shifted to make it compatible with the

dual gate MOSFET amplifiers. The circuitry for conditioning the AGC control signal is located on the first downconversion mixer card.

#### 2.2.3.2 First RF Downconversion Mixer

A dual gate mixer MOSFET, type RCA 40823, is used as an active mixer for the downconversion from 70 MHz to 10.7 MHz. The 70 MHz signal is applied to one MOSFET gate and the 59.3 MHz local oscillator is applied to the second gate. These two signals mix within the MOSFET transistor and the sum and difference frequencies as well as the original signals are available at the mixer output. IF filtering after the mixer will selectively filter out all components except the difference frequency of 10.7 MHz.

#### 2.2.3.3 IF Filters and Switches

The IF filters are multipole filters centered at 10.7 MHz. This is a common IF frequency for receivers and standard, off the shelf components may thus be obtained for IF strips operating at this frequency. The 10 KHz wide filter is a stock item from several crystal filter vendors, while the 100 KHz wide filter is a special order item from crystal filter vendors due to its wider bandwidth.

Switching signal paths at several MHz is difficult when

using common toggle or rotary switches due to poor isolation and VSWR of the switches. The scheme used here has only DC current flowing through the switch contacts and permits the use of inexpensive switches to control the RF path. A DC voltage controlled by the toggle switch is used to bias diodes in the signal path either forward or backward. When biased in the forward direction they present a low impedance and close an RF path, but when reverse biased, they present a high impedance and open circuit the RF path.

#### 2.2.3.4 10.7 MHz Amplifier Limiter

The 10.7 MHz limiter is implemented with a multiple stage differential amplifier that is driven into saturation. A constant current source in the emitter supply of the last stage limits the output current available and thus the output voltage is limited. An RCA CA3076 integrated circuit performs this limiting function in very small package size.

#### 2.2.3.5 Modified Costas Carrier Loop

The overall block diagram of the modified Costas carrier loop is shown in Figure 43 of section 2.1.4.1 and a detailed block diagram with actual signal flow interconnections is entitled as CXR Loop, 5-7, in the accompanying data package. Five functional modules are used in the modified Costas carrier loop, and are shown as follows in the CXR loop block diagram.

- A14 - I & Q mixers and  $90^\circ$  phase shifter
- A11 - I & Q limiters, third mixers, and summer
- A12 - Loop filter
- A13 - Acquisition indicator
- A17 - 10.7 MHz VCXO

Each of these modules contain circuits that are necessary to the operation of a modified Costas loop and will be discussed separately.

#### 2.2.3.5.1 A14 - Data Phase Detectors

The output of the 10.7 MHz limiter is applied to J15 the RF input of A14. The signal is amplified, buffered, and split by an RCA CA3028 differential amplifier followed by 2N918 transistors for impedance conversion. A standard double-balanced diode mixer is used in the I and Q channels for translating the signal to baseband via a 10.7 MHz VCXO. This local oscillator is applied to J16 where it is split and phase shifted by L27 and C64, each of which provides  $45^\circ$  of phase shift but in opposite directions when loaded by the CA3028 buffer circuitry. In this manner two L.O. signals in quadrature ( $90^\circ$ ) are obtained and applied to the I and Q mixers. The two baseband signals thus obtained are low pass filtered to remove the 10.7 MHz L.O. feedthrough component and the 21.4 MHz upper sideband present at the mixer output. A wideband buffer amplifier then scales the mixer output voltage by a factor of 16 and provides current

boosting capability to drive circuits following the data phase detector. The buffer used for this purpose is an RCA CA3026 with 2N2222 transistors acting as current amplifiers within a feedback loop. Peak-to-peak output voltage at the I and Q buffer outputs is about 9 volts, corresponding to .56 volts peak-to-peak out of the I and Q mixers. Since this 9 volts occurs over  $180^\circ$  or  $\pi$  radians, the I and Q phase detector gain  $K_o$  is  $9V/\pi$  radian = 2.86 V/radian. This value will be used in later calculations involving the loop filter and VCXO.

#### 2.2.3.5.2 All - Baseband Phase Detector

The I and Q signals are each routed to three items on the baseband phase detector or third mixer board. The first and second items are two buffers with gains of plus one and minus one respectively, and their outputs are connected to a FET switch used as a third mixer. The last item connected to the I and Q inputs is a limiter which makes a hard decision as to symbol polarity and drives the FET switches of the opposite channel accordingly. Overall gain of the board is one and offset voltage is near zero volts since an NPN buffer precedes a PNP buffer and their base emitter voltages cancel each other. An NE531V op-amp is used as a summer for the I and Q third mixer outputs. A FET switch appears in series with the I third mixer output so this switch is closed for SQPSK and open for BPSK

operation.

A significant feature of this board is that no low pass filter with a cutoff at the bit rate is present before the third mixer or limiter. No low pass is required in this situation since the IF filter has already been optimized to the data rate, and switching is done on the IF filters rather than on low pass filters at baseband. This implementation allows small dynamic range mixers to be employed.

#### 2.2.3.5.3 A12 - CXR Loop Filter

The loop filter board has two sets of loop filters, one set of wide bandwidth filters for initial acquisition and another set of narrow bandwidth filters for optimum reference carrier extraction once the loop is locked to the incoming signal. Three different loop filters are included in each set of filters and one of these three loop filters is selected according to the data rate and demodulation mode chosen. Since we are only interested in two data rates, 10 KBPS and 100 KBPS, plus a single demodulation mode, SQPSK, only two loop filters will be necessary for correct operation.

According to equation 24 in section 1.4.2.8 the IF bandwidth should be approximately 1000 times the loop bandwidth for a 30 dB improvement of reference carrier SNR in the loop. Since the threshold of most modems is in the range between 0 dB  $E_b/N_0$  and 10 dB  $E_b/N_0$ , this implies a minimum loop SNR

of 30 dB to 40 dB, an adequate number for most applications. For the 10 KHz IF bandwidth one should have a loop bandwidth near 10 Hz, and about a 100 Hz loop bandwidth for the 100 KHz IF filter. When in the initial acquisition mode the loop bandwidth is widened to approximately ten times the tracking bandwidths described above.

A significant feature of the switching process in changing from wide loop bandwidth to narrow is that the voltage on each loop filter capacitor is equal before switchover takes place. This assures that no large voltage step will occur in the loop which would tend to throw it out of lock at the time of changeover.

An amplifier with a voltage gain of 2.5 follows the passive loop filters and acts as a buffer for the loop filter output voltage to the 10.7 MHz VCXO. Summed into this amplifier along with the loop filter voltage is a sawtooth sweep voltage to increase the range of carrier loop acquisition. The sawtooth is generated on A7 during initial acquisition and is shut off by the same signal that changes the loop filters from wide to narrow. This signal is derived on A13, the lock detector board, and is an indication that carrier lock has been obtained. The sweep circuit may also be manually disabled on A13 by means of a jumper wire.

#### 2.2.3.5.4 A13 - Lock Detector Board

Both the inverted and noninverted I and Q signals from the baseband phase detector board (A11) are rectified and then applied to level comparators for BPSK operation and window comparators for QPSK operation. The output of the comparators is low pass filtered and the result compared against a set threshold to determine whether the carrier loop is locked or not. A bit timing lock indicator is also generated by ANDing the CXR lock and BIT locks together.

#### 2.2.3.5.5 A17 - 10.7 MHz VCXO

The 10.7 MHz VCXO is enclosed in an 85°C oven for stability and uses a 2N918 transistor oscillator and an RCA CA3028 buffer stage. The 10.7 MHz VCXO output is transformed down from the CA3028 high impedance output to a 50 ohm impedance. Frequency deviation of the VCXO is 1 KHz for a .83 volt input change. This determines the VCXO gain which is:

$$K_O = \frac{1000 \times 2\pi \text{ rad/sec}}{.83 \text{ volt}}$$

$$K_O = 7570 \frac{\text{rad/sec}}{\text{volt}}$$

#### 2.2.3.6 Bit Timing Loop and Data Detection

A detailed block diagram of the bit timing loop and data detection circuits is contained in the "Wiring Diagram - Integrate and Dump, Bit Loop, and Diff Decoder" interconnection diagram in the accompanying data package. The major functional blocks are as follows:

- A10 - Integrate and Dump
- A42 - Data Transition Detector
- A9 - Bit Loop Board
- A8 - Clock, Diff Decoder
- A7 - Demodulator Interface

These five modules will be discussed separately.

##### 2.2.3.6.1 A10 - Integrate and Dump

The I and Q baseband signals are each applied to a limiter and an integrator on the A10 board. A FET switch is used to dump the integrator to zero volts at the end of each symbol period, as established by the bit timing loop, and the same timing signal is used to sample and store the integrator output immediately before it is reset to zero. The stored version of the previous bit is then exclusive OR-ed with the real time version of the present bit at the output of the limiter. This signal is then used on A9 to generate a bit timing loop acquisition indicator. The hard limiter output goes to A42, the data transition detector board.

#### 2.2.3.6.2 A42 - Data Transition Detector

The data transition detector accepts a hard limited version of I and Q channels from the A10 Integrate and Dump board. Narrow pulses are then generated to define the rising and falling edges, or data transitions in the I and Q channels. These pulses trigger I and Q one shots which are adjusted to provide a pulse duration of one half a symbol period. Bit rate and demodulation mode inputs control the one shot pulse time.

#### 2.2.3.6.3 A9 - Bit Loop Board

The bit loop board contains I and Q phase detectors, a loop filter, bit timing VCO, and an acquisition indicator. The bit timing and acquisition phase detectors are implemented with digital exclusive OR gates whose I and Q outputs are resistively summed to provide either AFC or acquisition information. Switchable low pass filters smooth the acquisition information before a threshold comparator decides whether the bit timing loop is locked. This output is logically ANDed with the carrier lock indication on the Lock Detector board, A13, and the resultant output is the bit lock indication.

Bit timing AFC information is filtered by a passive loop filter which is switched according to data rate. A buffer amplifier scales this signal and level shifts it to be compatible with an RC voltage controlled oscillator. An

NE566V function generator is used as the 400 KHz bit timing VCO since it has an FM capability.

#### 2.2.3.6.4 A8 - Clock, Diff Decoder

The clock divider circuits to generate the correct bit rate clock and associated waveforms for demodulator operation are located on this circuit card. The 400 KHz VCO output from A9 is buffered and divided by two to produce a symmetrical square wave at 200 KHz. This square wave is then routed to a final divide by two to produce a 100 KHz clock signal. When operating at 10 KBPS a divide by ten circuit is switched in between the 200 KHz signal and the final divide by two so that the final output is 10 KHz. The final divide by two is used for SQPSK operation only and is switched out for BPSK decoding.

The final clock signal is routed to two flip-flops which generate two 50 KHz (or 5 KHz) signals that are 90° out of phase. These signals provide timing for the staggered I and Q data channels to sample the integrators and reset them to zero. Once the I and Q outputs have been sampled and differentially decoded on this board they can be recombined into a serial bit stream with the gating arrangement shown in the schematic. For BPSK this recombination is unnecessary because data is only present in the I channel and so the recombination circuitry is bypassed in that mode of operation.

#### 2.2.3.6.5 A7 - Demodulator Interface

The demodulator interface has TTL to EIA converters for clock and data lines going to the external world. These change the 0V to 5V logic levels to  $\pm 6$  volt output levels. The buffers placed on this card must of course be compatible with any equipment intended to process demodulated data.

Also contained on this board is a sweep circuit for carrier acquisition and interface for a built-in error counter.

#### 2.2.4 Performance Estimates

The following analyses and discussions detail the expected operation and performance of the specific 10 KBPS/100 KBPS modem presented.

##### 2.2.4.1 Carrier Loop

The carrier loop is a high gain second order loop employing a passive loop filter. Since it is high gain and  $\omega_n/K_oK_d \ll 2\zeta$  one may use the simplified equation 22 for representing loop performance rather than equation 23.

Loop gain is the first quantity to be calculated, and the simplified carrier loop shown in Figure 56 will help visualize the quantities involved.

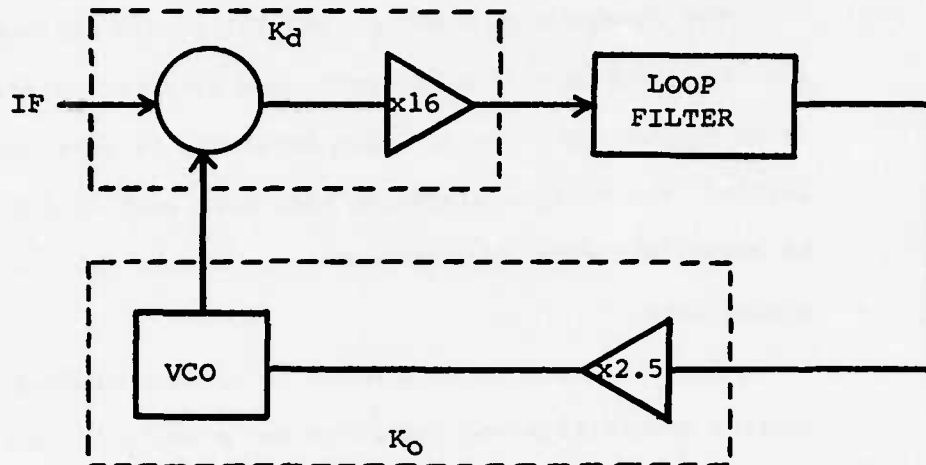


Figure 56. Simplified Carrier Loop

Phase detector gain has already been calculated as

$K_d = 2.86 \text{ Volts/radian}$  and this includes the x16 buffer.

VCO gain has been determined but we now need to include the x2.5 buffer on the loop filter board as part of the VCO gain. The overall result is:

$$K_o = \frac{2\pi (1000) \text{ rad/sec}}{.83\text{V}} \times 2.5$$

$$K_o = 18,925 \frac{\text{rad/sec}}{\text{volt}}$$

Thus, the loop gain is:

$$K_v = K_o K_d$$

$$K_v = (2.8 \frac{\text{volts}}{\text{radian}}) (18,925 \frac{\text{rad/sec}}{\text{volt}})$$

$$K_v = 54,126 \frac{1}{\text{sec}}$$

Assuming a 1 KHz total offset frequency one may now calculate a static phase error for the loop from equation 26 as follows:

$$\theta_v = \frac{\Delta\omega}{K_v}$$

$$\theta_v = \frac{2\pi(1000)}{54,126}$$

$$\theta_v = .12 \text{ radians}$$

$$\theta_v = 6.63^\circ$$

The above procedure is of course backwards from the initial design approach as shown in section 2.1.4.2.8 since we are dealing with specific components and analyzing their performance. The static phase error obtained is a reasonably small number and will contribute a negligible degradation.

The second quantity to determine is the loop filter and this can be done by the graphical method of section 2.1.4.2.8 since we know  $K_v$ ,  $\omega_n$ , and will choose  $Z \approx 1$ . Having done this one must pick standard component values to implement the loop filter. Since these are inexact we can now recalculate  $\omega_n$  and  $Z$  to verify the accuracy of our graphical analysis and component selection. The results of the calculations are as follows:

ITEM	10 KBPS	100 KBPS
$\omega_n = \sqrt{\frac{K_v}{T_1 T_2}}$	15.9 Hz	65 Hz
$Z = \omega_n T_1 T_2 / 2$	.982	.952
$T_1$	.0292 Hz	.482 Hz
$T_2$	8.08 Hz	33.8 Hz

These values of  $\omega_n$  are near the desired bandwidths of 10 Hz and 100 Hz, the damping factor is close to one so the design of the carrier loop is satisfactory.

#### 2.2.4.2 Bit Timing Loop

The bit timing loop analysis is exactly identical to the carrier loop analysis. Loop bandwidths of approximately 60 Hz for 10 KBPS and 250 Hz for 100 KBPS operation are obtained in the final design.

#### 2.2.4.3 Data Detection

Since the specific case is a modification of an existing modem one may readily predict performance based on measured results of the predecessor. The original modem worked at 1/3 the data rate of the modified demodulator so the modification should have roughly three times the degradation of the original modem. Because the original modem was less than 1 dB from theoretical the modification should be less than 3 dB from theoretical.

Most bit error rate degradations are easily analyzed in the time domain because of the linear integrate and dump characteristics. Loss of signal due to finite dump pulse width and bit timing error is expressed by the following relationship:

$$L = 20 \log \left( 1 - \frac{\gamma}{T} \right) \quad \text{EQ. 27}$$

Where:

$L$  =  $E_b/N_0$  loss in dB

$\gamma$  = Timing error plus dump pulse width

$T$  = Symbol period

Thus, for a dump pulse width of 1  $\mu$ sec and a timing error of 1  $\mu$ sec with a 100 KBPS SQPSK data rate, one calculates about 1 dB of degradation from theoretical.

Additional degradation occurs in the prelimiting IF filter and this amounts to approximately 1 dB also.<sup>4</sup> The IF filter rejects a certain amount of signal energy and also causes phase distortion within its passband.

The total degradation from these two major effects is about 2 dB from theoretical.

#### 2.2.5 Operation of Demodulator

The demodulator would be operated by connecting a 70 MHz SQPSK signal to the input and selecting 10 KBPS or 100 KBPS according to the incoming data rate. The remaining switches would be set for SQPSK and differential decoding and then the serial EIA output connected to the user equipment.

#### 2.2.6 Modification of Demodulator

The demodulator design may be easily modified for different bit rates which are a sub-multiple of 100 KBPS or 10 KBPS by adding additional clock dividers and then changing both the carrier and bit timing loop filters where necessary. For bit rates that are nonintegral sub-multiples one must change the center frequency of operation of the bit timing VCO.

Modifications for functions other than SQPSK demodulation involve FM demodulation where information is taken from the VCO control line. It must be remembered that this line is at +3.6 VDC at center frequency and has a positive slope of .83 volts/KHz. The loop filter must be modified so the loop can track the fastest frequency change with small phase error and then the VCO line must be level shifted and scaled for the appropriate output function desired.

#### 2.2.7 Costs of Various Items

The most expensive components of demodulators are those having the toughest specifications and this is normally the VCXO and IF filters. The following approximate component costs are given to show the relative cost of implementing various functions.

VCXO		\$103.60 Built
Ø Detector		\$ 10.00
Ø Shifter		\$ .50
IF Filters	10 KHz	\$ 45.00 to \$144.00
	100 KHz	\$175.00 to \$288.00

From this list one may readily ascertain that components involving crystals and crystal technology far exceed the cost of all other components in a typical PSK demodulator. One should also note that a packaged VCXO could cost up to ten times the price of assembling the same item from scratch, and that an average cost of \$300 to \$500 is reasonable for this component if purchased as a unit.

IF filters with a percentage bandwidth between .1% and .3% of center frequency can be obtained cheaply if the desired item is a standard center frequency and bandwidth, and the 10KHz filter falls into this category. The 100KHz is a special wideband filter of about 1% bandwidth and costs considerably more. Possible vendors for these items are Heath Dynamics and Tyco Filters.

## 2.3

CONCLUSIONS

A modified Costas loop has shown itself to be an effective means of providing a reference carrier estimate in multiple data rate demodulators. It can be easily constructed

to handle BPSK, QPSK, or SQPSK modulated signals, as well as FM voice and FSK detection. The modified Costas loop does not demodulate data, however, and one must also implement a bit timing loop and a data detection circuit in order to obtain usable digital data.

## 2.4

RECOMMENDATIONS

Subject areas for further study relating to Costas loops and PSK demodulators have been encountered during this effort. The following list is a general description of these topics.

1. True data aided carrier loops.
2. Loop analysis and computer simulation in the presence of noise.
3. Implementation study of various bit timing loops including digital versus analog.
4. Theoretical and implementation study of digital versus analog carrier loops.

References

- <sup>1</sup>S.A. Rhodes, "Effects of Hardlimiting on Bandlimited Transmissions with Conventional and Offset QPSK Modulation," National Telecommunications Conference, December, 1972, I.E.E.E. Publication 72CHO 601-5-NTC, Page 20F-1.
- <sup>2</sup>Mischa Schwartz, Information Transmission, Modulation, and Noise, McGraw-Hill Book Company, @ 1959, 1970.
- <sup>3</sup>Floyd M. Gardner, Phaselock Techniques, John Wiley & Sons, Inc. @ 1966.
- <sup>4</sup>J. J. Jones, "Filter Distortion and Intersymbol Interference Effects on PSK Signals," I.E.E.E. Transactions on Communication Technology, Vol. COM-19, No. 2, April, 1971.

## SECTION III

## TUNED AMPLIFIERS

## 3.1 GENERAL CASE

3.1.1 General Requirements

A set of tuned amplifiers were required that could be used in the configuration of a MODEM. These amplifiers were to use a building block approach. This would allow various gains, bandwidths, and isolation to be selected by changing the combination of blocks.

The amplifiers were given a set of general requirements and a set of specific requirements. The general requirements cover a range of operating characteristics while the specific requirements are for specific gains, bandwidths, and operating frequency.

The general requirements were given to provide the capability of possible operation within a range of characteristics. This operation would be obtained from the units built by either retuning or minor modification. The modifications would be a change of component value. The general requirements are: an operating frequency of 60 MHz to 80 MHz, bandwidths of 1 MHz to 40 MHz, gains of 0dB to 50dB, reverse isolation of 70dB, output capability of +18dBm, and a 50 ohm input and output. The gains are to be manually selectable in 10dB steps and there would be an AGC capability with a .02 to .04 volt/dB sensitivity over a 55dB range. The specific requirements are for deliverable units, and are distinct characteristics within the general

requirements. These specifications for five different amplifier types are given in 3.2.1.

### 3.1.2 Amplifier Methods And Implementations

In selecting an amplifier that would meet the requirements consideration was given to; linear integrated circuits (IC's), discrete component, hybrid circuit, and modular amplifiers.

Any of these amplifiers could provide the desired characteristics, but there is a difference in the degree of complexity to implement them. To obtain flexibility and simplicity, as well as meet the requirements, consideration must be given to the implementation.

To implement a linear IC amplifier requires the addition of resonant circuits at the input and the output of the IC. They require a small number of discrete components to select the operating frequency, the gain, and to match the input and output to 50 ohms. A means of interconnection of components can be accomplished by mounting the circuitry on a printed circuit board (PCB).

A discrete component amplifier requires a transistor with its associated bias and resonant circuits. The bias circuitry sets a dC operating point, and the resonant circuits select frequency, set a gain, and match the input and output. These circuits require only a small number of components. An interconnection of the components can be done on a PCB.

The hybrid circuit amplifier like the discrete component

amplifier is a combination of passive components with an active device. These components are chip capacitors and active devices, film resistors, and chip or small wound inductors. The actual implementation is then accomplished by bonding the components to a ceramic substance. The complete amplifier is then enclosed in a small package.

Modular amplifiers are self contained units that require no external circuitry. Only input power is needed to operate.

### 3.1.3 Advantages and Limitations of the Various Methods

Examination of the advantages and limitations was used in the selection of an amplifier. This determined which method would best fit the requirements. The advantages and limitations of each method are as follows:

The MC1590G, a linear IC, has the advantages of high gain capability, is gain controllable, requires relatively few discrete components, is easily modified, and is low cost. It has limitations in output level since 0dBm is about the maximum obtainable, and it is size limited by the area needed for the discrete components.

The discrete component amplifier has the advantages of high gain, good reverse isolation, flexibility of design, easily modified, high output power capability, low cost, and the components are readily available. It has the disadvantage that size reduction is limited by the area required by the discrete components. If a very small size is necessary, degradation of amplifier performance occurs.

As a rule for an rf stage, 30 dB isolation can be achieved. Reverse isolation of a transistor stage can be determined by the Y parameters of an amplifier. If 70 dB is required, two or more stages will be needed. One unity gain stage will provide 50 dB of isolation (20 dB gain, 20 dB pad, and 30 dB natural stage isolation). It can be seen that to meet 70 dB of isolation a fair amount of complexity is required which requires a larger package. Since size is important, a tradeoff will be made between isolation and size with a smaller size selected in place of isolation. In most cases isolation of 70 dB is not necessary.

Another area of consideration is that of noise figure. For a receiver system the cascaded noise figure is:

$$NF_{TOT} = \sum NF_1 + \frac{NF_2}{G_1} + \frac{NF_3}{G_2 G_1} + \dots$$

It can be seen that with moderate to high gain in the first stage, the noise figure will primarily be determined by the first stage with lesser contributions by each succeeding stage. Normal receiver design techniques provide for a moderate gain low noise front end as required. Subsequent stages, therefore, need not be designed for very low noise. However, a general rule is that the noise figure should not exceed 15 dB.

The hybrid amplifier has one major advantage in its very small size. This amplifier also can be designed for a wide range of operating characteristics. Its disadvantage is high cost in the development of it. This amplifier also does not lend itself to modification and is limited in power output by how much heat the package can safely dissipate.

The modular amplifier has the advantage of requiring no external circuitry. They offer broadband operation and can be obtained in small packages. Its disadvantages are comparatively low reverse isolation, usually cannot be modified, and they usually have lower gain.

Considering the characteristics of each amplifier method, a combination of discrete amplifiers and linear IC amplifiers will provide the best compliance to the requirements. These methods will provide flexibility in both design and operation. They are also low cost methods to build and maintain, and are easily modified to the general requirements.

### 3.2 THE SPECIFIC CASE

#### 3.2.1 Specific Case Specifications and Requirements

The requirements for the five deliverable amplifiers have specific gains, bandwidths, and operating frequency. In the specific case some deviation occurs from the general requirements. The reverse isolation of 70dB cannot be expected from a single amplifier stage. To provide a minimum physical size the general requirement was modified.

In considering the intended use for the amplifiers it was determined the +18dBm output level was not needed. A +10dBm level would require much less input power and will provide sufficient power for the intended use.

The individual amplifier requirements are as follows:

- A) A Buffer Amplifier to provide isolation between successive stages was desired to have 70 MHz center frequency, 0dB gain, 50dB reverse isolation, provide a +10dBm output level, and operate in a 50 ohm system with less than a 2.0:1 VSWR. An original requirement for 1 MHz bandwidth was changed to allow use of a 20 MHz bandwidth amplifier stage without a filter. The reasons for the change were to reduce package size and provide for more versatile use of the buffer. By allowing a wider bandwidth the buffer amplifier may be used with the offset amplifier at 73.8 MHz as well as with the amplifiers at 70 MHz. When required, the narrow bandwidth would be more useful if it is a separate filter.
- B) A Broadband Amplifier was desired that would have 10dB of gain, 40 MHz bandwidth, provide a +10dBm output level, have 30dB of reverse isolation, and operate in a 50-ohm system with less than 2.0:1 VSWR.
- C) A Medium Gain Amplifier, 73.8 MHz, was required that would operate at center frequency of 73.8 MHz, have 30dB of gain, 2 MHz bandwidth, provide a +10dBm of output power, and operate in a 50-ohm system with less than a 2.0:1 VSWR. The

design goal of 70dB reverse isolation was not achieved due to the cross coupling discussed in Section 3.2.3 (C), and transistor parameter variations that are discussed in Section 3.2.3 (A). A reverse isolation of 60dB was obtained and is considered satisfactory since one criterion for reverse isolation is that it be greater than the forward gain. This prevents instability due to feedback. Another consideration for reverse isolation is for rejection at the input to unwanted signals occurring at the output. These signals would probably be mixer spurious and considering the levels at which they might be results in levels 80dB down or less with 60dB reverse isolation. This begins to reach the isolation possibilities of the cables external to the amplifier unit, and therefore, greater internal reverse isolation would not be of much benefit.

The bandwidth of this unit came out 1.5 MHz which is somewhat narrower than the goal of 2 MHz. This is satisfactory since it will allow a one-megabit data rate, which is in line with the intended use. It will also provide a little more rejection outside the passband.

D) The Medium Gain Amplifier, 70 MHz, had the requirements of 70 MHz center frequency, 30dB of gain, a 10 MHz bandwidth, 70dB of reverse isolation, provide a +10dBm of output power and operate with less than 2.0:1 VSWR in a 50-ohm system.

E) The IF Amplifier was required to operate at a center frequency of 70 MHz, have 50dB of gain, 70dB of reverse

isolation, 55dB of AGC range with an AGC sensitivity of .02 to .04 volts/dB, provide a +10dBm of output power, and operate with less than 2.0:1 VSWR in a 50-ohm system. An original requirement for a 1 MHz bandwidth on this unit was changed and allowed to be approximately 7 MHz. Relaxing the bandwidth requirement follows the same discussion as Section 3.2.1 (A) in that a smaller, more versatile unit can be obtained.

### 3.2.2 Description of Scheme Used

To provide the individual specifications of the previous section, single-stage amplifiers, attenuators, and bandpass filters have been arranged in varying combinations. For the five amplifier units a description of the scheme used is given through the use of block diagrams and their analysis.

#### (1) Buffer Amplifier:



Figure 57. Buffer Amplifier, Block Diagram

The buffer amplifier utilizes an amplifier preceded by an attenuator to provide the requirements of Section 3.2.1(A).

The basis of the buffer amplifier is a single-stage transistor amplifier. An amplifier of this type is capable of 20dB gain and reverse isolation of up to 30dB. With this amplifier it is also possible to provide the output power, bandwidth and VSWR requirements.

The attenuator precedes the amplifier so that approximately a 20dB pad may be used to reduce the gain and increase

the reverse isolation while not interfering with the power output capabilities of the amplifier.

(2) Broadband Amplifier:

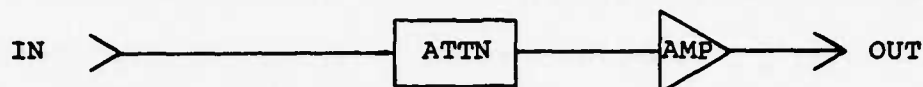


Figure 58. Broadband Amplifier, Block Diagram  
The broadband amplifier uses the same basic scheme as

the buffer amplifier to meet its requirements. The attenuator was reduced to provide the 10dB gain, and the output coupling changed from capacitive to transformer. The transformer coupling will provide the wider bandwidth desired for this unit.

(3) Medium Gain Amplifier (73.8 MHz):

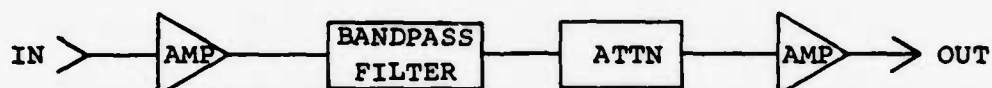


Figure 59. 73.8 MHz Medium Gain Amplifier, Block Diagram  
The medium gain amplifier is offset to a center frequency

of 73.8 MHz and uses two stages of gain, a bandpass filter, and an attenuator to meet its requirements. The amplifier stages are of the same design as in the buffer amplifier. Since their bandwidth is much wider than the requirement for this unit, the selectivity is accomplished with a bandpass filter. The bandpass filter not only provides the desired narrow bandwidth, but also provides much greater attenuation of frequencies outside the passband than can be accomplished with the tuned amplifier.

In addition to the insertion loss of the filter, an attenuator

is included to further reduce the gain to 30dB. The attenuator also provides a resistive termination to the filter and the input of the last amplifier stage. The resistive termination greatly reduces the possibility of instabilities caused by reactive loads as well as improving consistency in unit-to-unit operation.

(4) Medium Gain Amplifier (70 MHz):

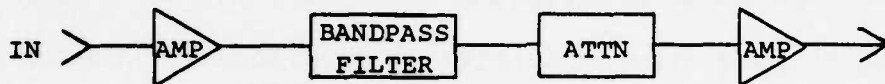


Figure 60. 70 MHz Medium Gain Amplifier, Block Diagram  
The scheme used for this amplifier is the same as the previous unit in Section 3.2.2 (3) since the requirements are the same except for center frequency and bandwidth.

The bandpass filter selects the frequency response for the 10 MHz bandwidth which, is a greater percentage of the center frequency. This is a larger percentage bandwidth, and results in a lower filter insertion loss. The lower insertion loss is compensated by increasing the attention of the pad to meet the gain requirements.

(5) IF Amplifier:

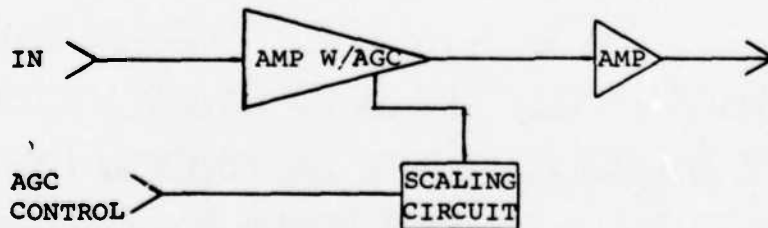


Figure 61. IF Amplifier, Block Diagram

The IF amplifier uses an amplifier with AGC capability, a circuit to regulate the AGC, and a single stage amplifier

to obtain the high gain and AGC range desired.

The first amplifier, a MC1590G, provides a 55dB AGC range, while combining with the single stage amplifier to provide 50dB of gain.

The scaling circuit is used to set the MC1590G gain to an area of relatively linear AGC operation and to control the sensitivity to the required .02 to .04 volts/dB.

The output stage is the same 70 MHz amplifier that has been used in the previous units.

### 3.2.3 Discussion of Schematics, Circuits, and Hardware

A) The Buffer Amplifier schematic, component location, parts listing, and assembly instructions are shown in Drawing 61-02230-001.

The attenuator section consisting of R5, R6, and R7 is a symmetrical Pi pad with a characteristics 50 ohm impedance (see Figure 62). The amplifier stage, consisting of Q1 and its associated circuitry, is matched to 50 ohms through C1 at the input and C6 at the output. Resistor R4 provides a resistive load to the collector of Q1 that insures circuit stability and presents a more constant impedance to the matching network. The matching network can then make the transformation to 50 ohms more reliably when subjected to unit-to-unit component value and transistor parameter variations.

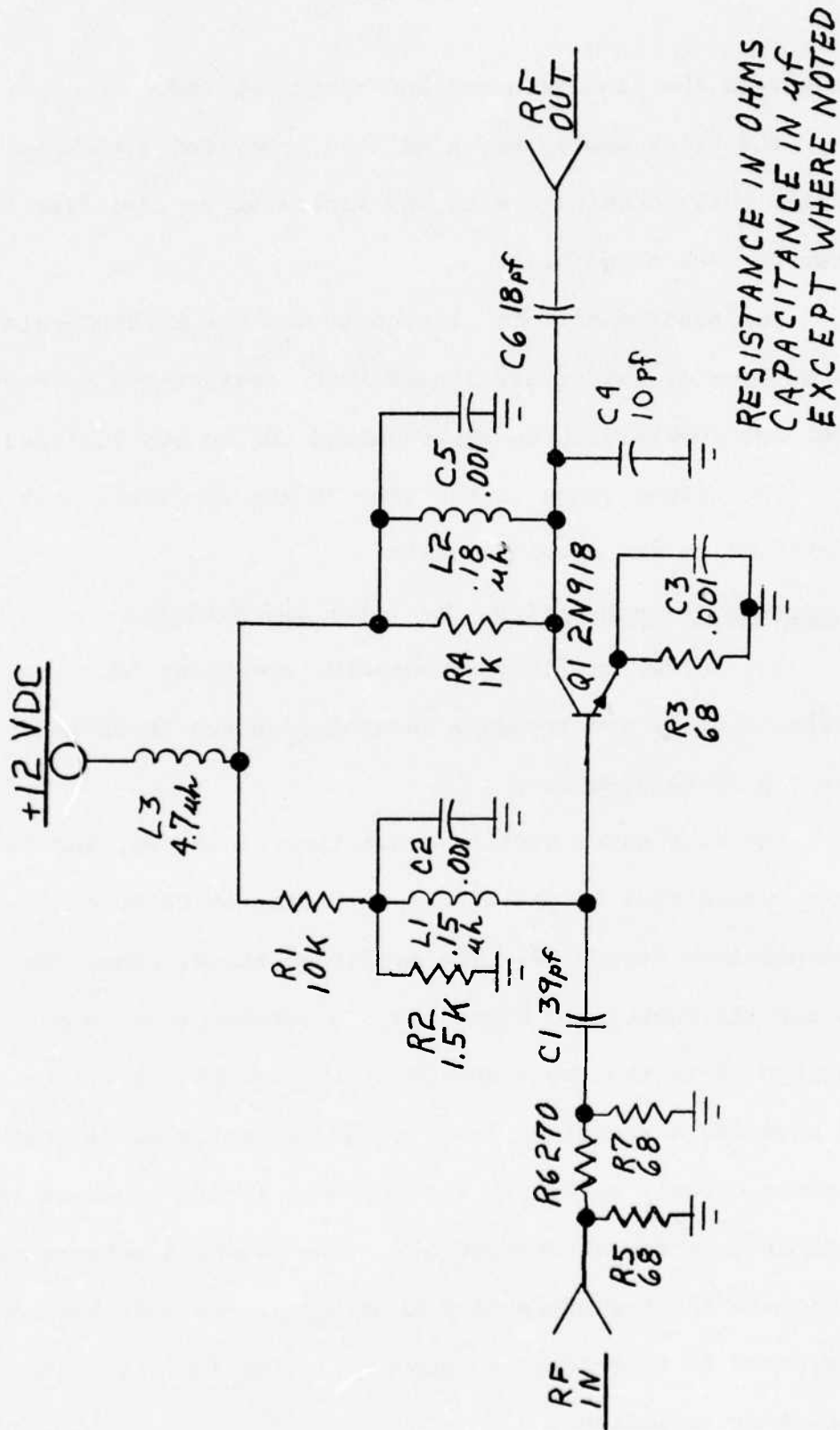


Figure 62. Buffer Amplifier, Schematic Diagram

Some difficulty was encountered with the reverse isolation of the amplifier stages when it was discovered they were not meeting the expected level of 30dB. Investigation found the  $C_{ob}$  of the 2N918 transistor to vary from device to device. This caused a variation in the reverse isolation that could be obtained. Manufacturer's specifications state a maximum  $C_{ob}$  of 1.5pf which in an amplifier circuit results in approximately 25dB of reverse isolation while the devices that would provide 30dB of reverse isolation were found to have a  $C_{ob}$  of less than 1.0pf. The reverse isolation, as a function of  $C_{ob}$ , then changed with reasonable linearity between the two points. However no major difficulty was encountered with obtaining the reverse isolation of the buffer amplifier. The amplifier stage generally had gains of 1 to 2dB higher than the expected 20dB, and most transistors were not at the maximum  $C_{ob}$ . With slightly higher amplifier gains the attenuator could be increased to obtain the 0dB unit gain, and simultaneously increase the unit's reverse isolation.

B) The Broadband Amplifier schematic, parts listing, component locations, and assembly information are shown in Drawing 61-02229-001.

The broadband amplifier (see Figure 63) has the same basic configuration as the buffer amplifier. With the

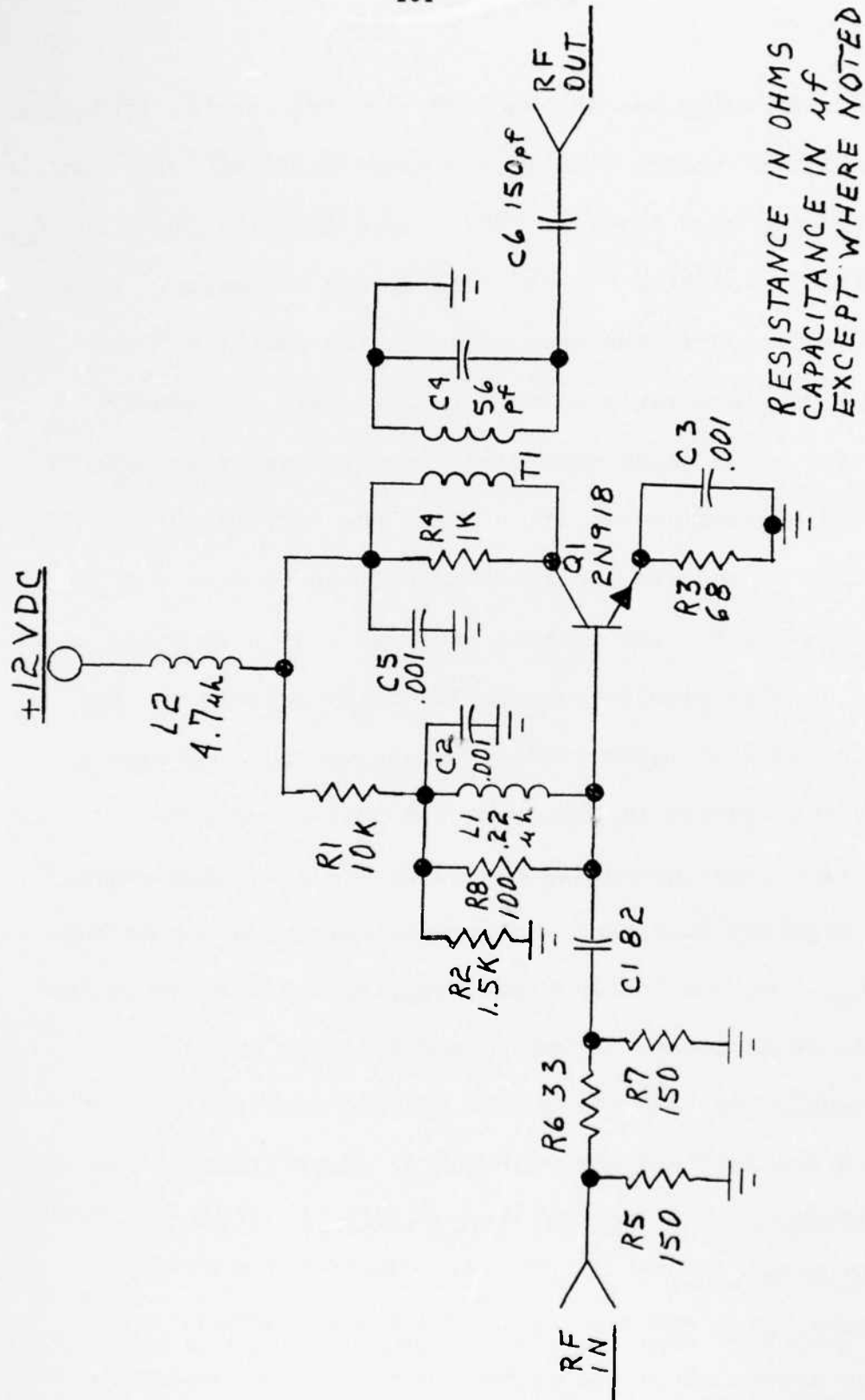


Figure 63. Broadband Amplifier, Schematic Diagram

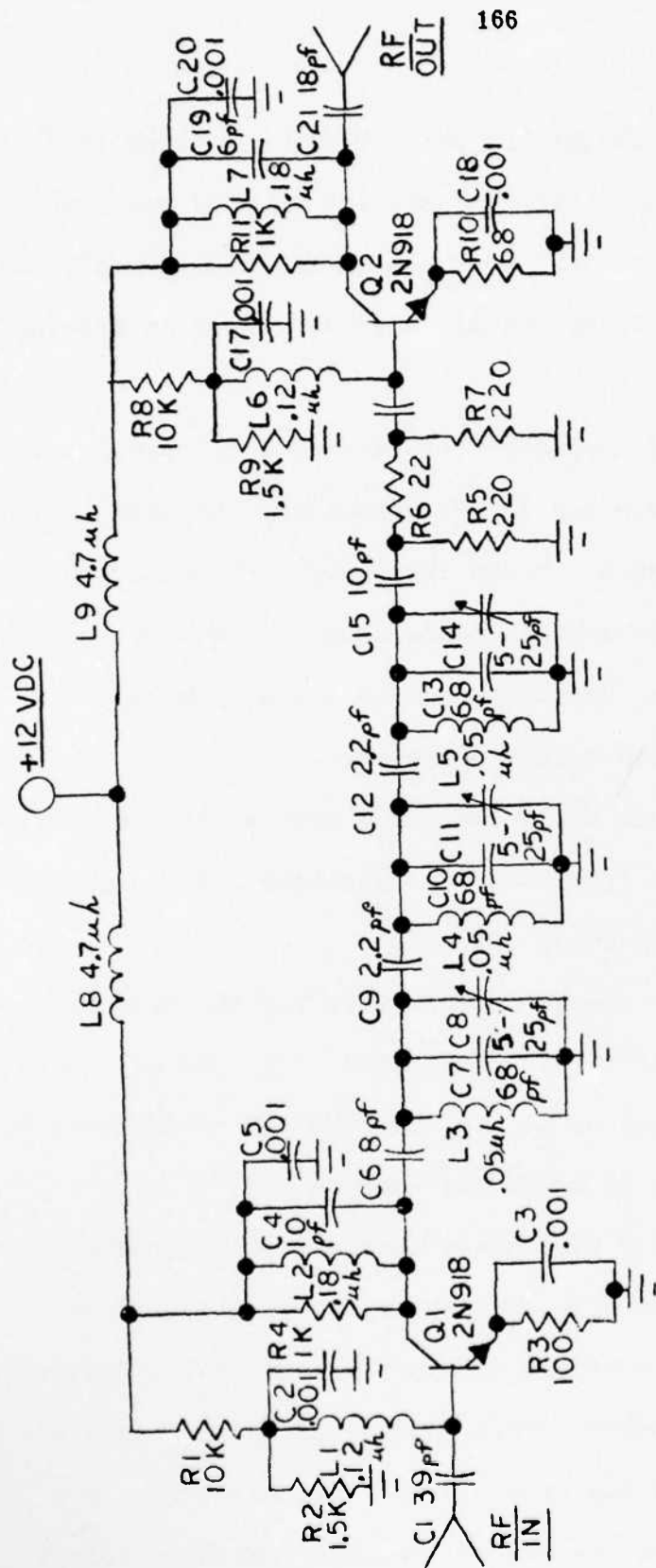
differences being slight, the printed circuit board (PCB) was constructed such that the same PCB is used for both amplifier units. To adapt for use in the buffer amplifier, it is only necessary to install wire W1, shown on Drawing 61-02230-001.

The broadband amplifier uses transformer coupling at the output to attain the 40 MHz bandwidth. It also includes Resistor R8 to insure a broad frequency response at the input that will not influence the output frequency response. Both the buffer and broadband amplifiers are packaged in 1.5 x 1.5 x 1.0 inch Modpak containers.

C) The Medium Gain Amplifier (73.8 MHz) schematic, parts listing, component locations, and assembly information are shown on Drawing 61-02232-001.

The amplifier stages in this unit are the same configuration as the amplifier in the buffer unit. It was necessary to change values on L1, L6, C4, and C19 to obtain a less than 2.0:1 VSWR at 73.8 MHz (see Figure 64).

The filter is a three-pole bandpass with parallel resonant L-C tank circuits and capacitive coupling. The capacitive coupling offers greater attenuation to frequencies below center frequency. This is desired for a possible application of the amplifier. The 2 MHz bandwidth is a small percentage of the center frequency which indicates



RESISTANCE IN OHMS  
 CAPACITANCE IN  $\mu$ f

Figure 64. 73.8 MHz Medium Gain Amplifier, Schematic Diagram

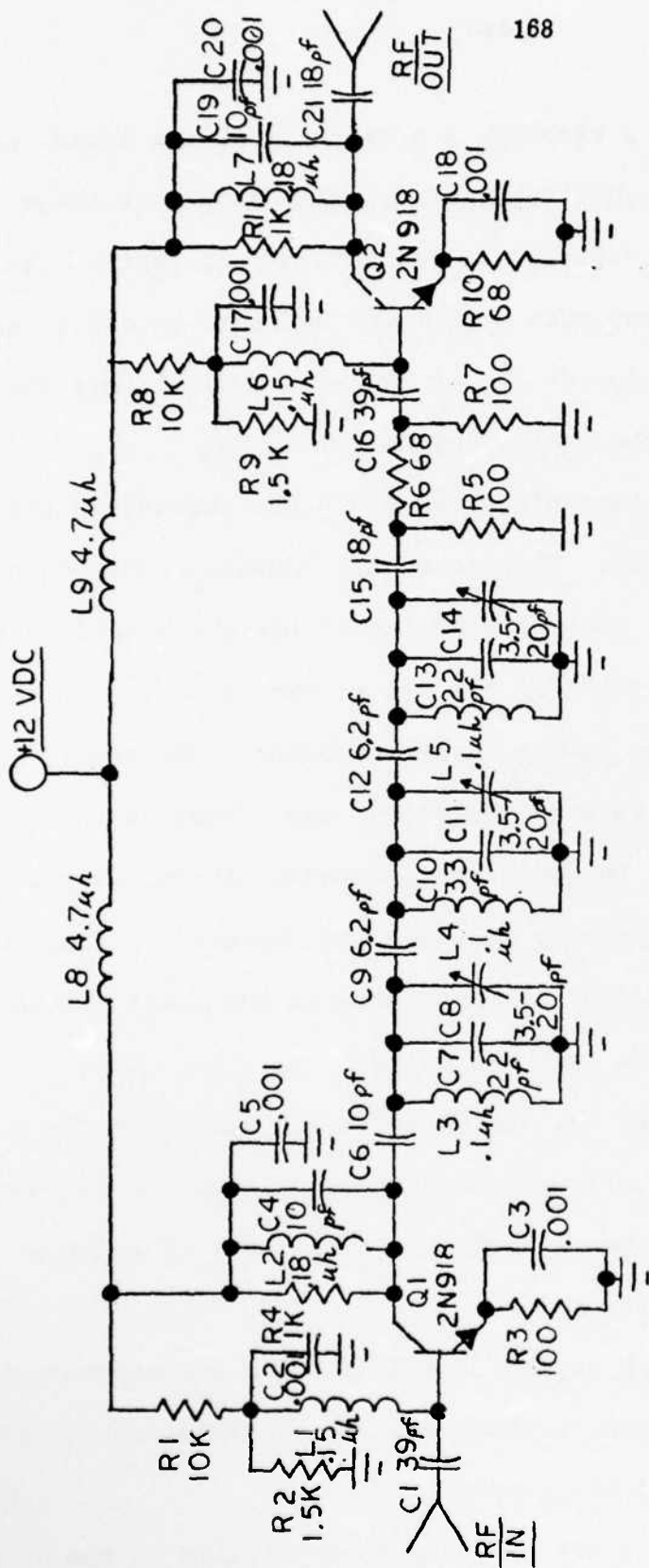
that, unless high Q elements are used the filter losses will be large. Since capacitors are normally high Q at these frequencies the inductors are the determining factor. In this filter the inductors were wound on metal toroid cores, and were able to provide a Q of 110 with a small physical size. This kept the filter losses below 10dB.

With a small percentage bandwidth the resonators are coupled very lightly. Therefore, any coupling other than through the signal path changes the filter characteristics. This effect was present in the filter due to radiation from the third resonator to the first resonator. The result was a decrease in the reverse isolation, and a bump in the frequency response below center frequency causing decreased rejection. The frequency response was improved by placing a brass shield between the components of the first and third resonators, as shown in the drawing.

The value of R3 was increased to 100 ohms from the 68 ohms used in the first amplifier stage in order to decrease the current requirement, since the high level of power is not necessary at that point.

D) The Medium Gain Amplifier (70 MHz) has the schematic, parts listing, component location, and assembly instructions shown on Drawing 61-02231-001.

The 70 MHz unit has the same configuration as the



RESISTANCE IN OHMS  
CAPACITANCE IN  $\mu f$

Figure 65. 70 MHz Medium Gain Amplifier, Schematic Diagram

73.8 MHz amplifier with a small difference in the component values (see Figure 65). The amplifier components in this case are the same as the buffer amplifier, and the filter components have been changed to provide a 10 MHz bandwidth at 70 MHz center frequency. Since the bandwidth is wider than the 73.8 MHz unit the coupling is not as critical and it was not necessary to include the brass shield. The larger percentage bandwidth also results in lower insertion loss which is offset by increasing the attenuation of the Pi pad, made up of R5, R6, and R7.

Because the configuration of the 70 MHz and 73.8 MHz medium gain amplifiers is the same, a common PCB can be used. The PCB assembly is mounted in a 1.5 x 3.25 x 1 inch Modpak container that is also common to both amplifier units.

E) The IF Amplifier has a schematic, parts listing, component location, and assembly instructions as shown on Drawing 61-02228-001.

The output amplifier is the same single stage that has been used in the previous units and provides the desired output power levels (see Figure 66). The AGC is accomplished through gain reduction of the MC1590G. The gain reduction is controlled by the value of resistor R7 and the voltage applied to R7. The value of R7 determines the voltage range and the linearity; the smaller R7 is the more linear the

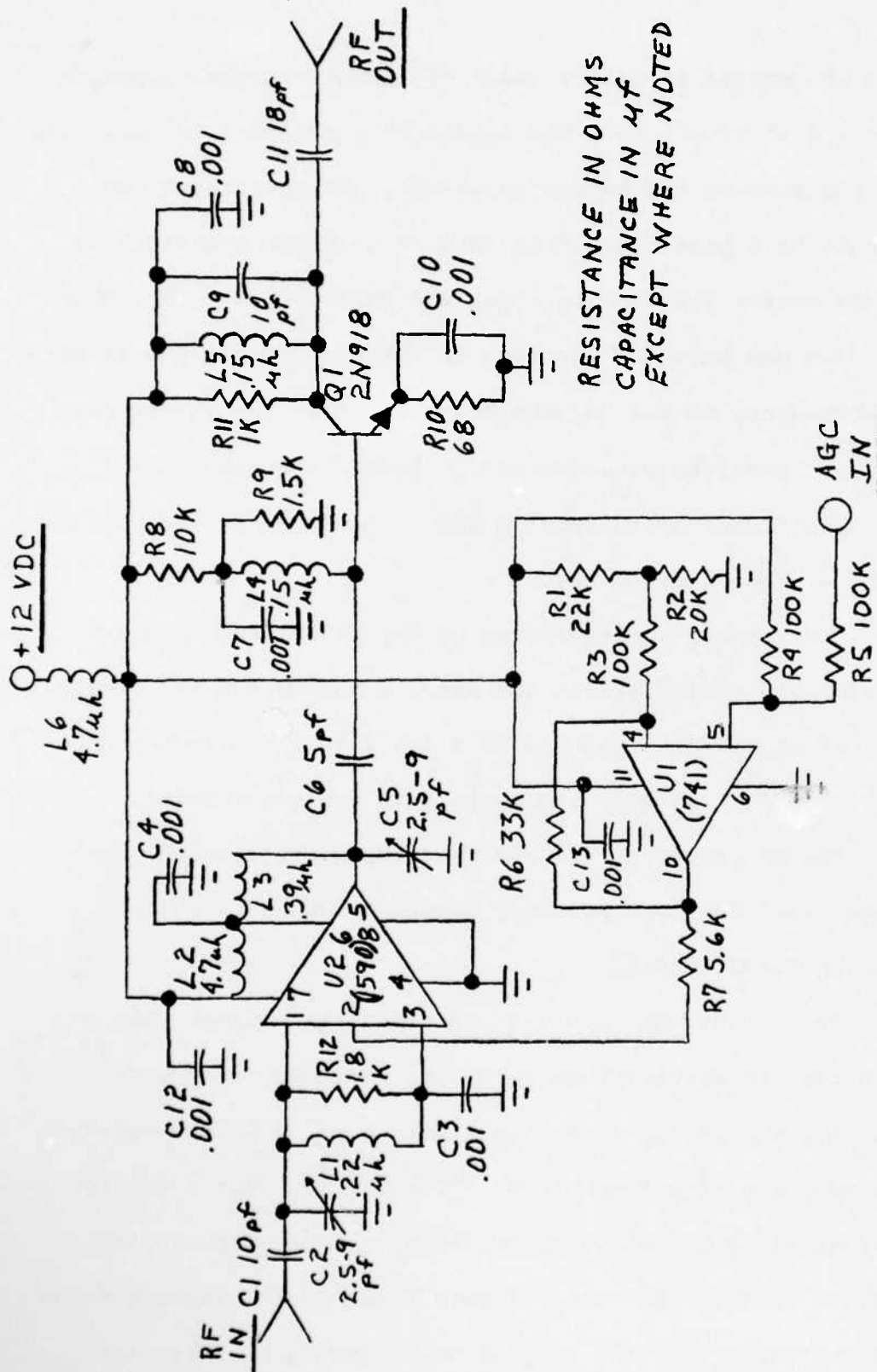


Figure 66. IF Amplifier, Schematic Diagram

AGC curve becomes and the less the voltage required for full gain reduction. U1, a 741 operational amplifier, translates the level and range required to obtain 55dB of gain reduction from the MC1590G and maintains a .02 to .04 volts/dB sensitivity at the AGC input. The AGC input is designed to operate between +1.5 volts and 0 volts. While it can be taken negatively, and will increase the gain, this is not recommended because the gain becomes greater than the reverse isolation creating a condition for oscillations. The negative voltage increases the gain since the MC1590G has been prebiased to move it to a linear point in the AGC curve.

It was necessary to provide a brass shield, as shown on the drawing, to prevent the feedback caused by radiation from the output to the input of the MC1590G. Finger stock also makes contact from the shield to the container wall to control the ground loops and primarily to prevent a feedback loop from the output of Q1 to the input of U2.

This amplifier unit is also contained in a 1.5 x 3.25 x 1 inch Modpak container. The packages of all the amplifier units are provided with an extended bottom cover to provide for convenient mounting.

#### 3.2.4 Data and Graphs

This section includes the actual data taken on each amplifier type listed by serial number. It includes data for

gain, reverse isolation, bandwidth, output power, VSWR, input power, AGC sensitivity and range, intercept point, and noise figure. Bandpass characteristics of the filtered units and AGC curves of the IF amplifier are also included.

Table 2. GAIN

	GOAL	1	2	3	4	5	6
BUFFER AMPLIFIER	0	0	0.3	0	0.5	0.7	0.5
BROADBAND AMPLIFIER	10	10.7	10.8	11.0	10.6	11.4	10.7
73.8 MHZ MEDIUM GAIN AMPLIFIER	30	30.1	30.4	31.2	30.7	29.8	31.2
70 MHZ MEDIUM GAIN AMPLIFIER	30	30.4	30.2	29.4	30.6	29.4	29.7
IF AMPLIFIER	50	52.0	49.0	50.2	48.7	51.5	51.7

MEASUREMENTS = DB

Table 3. REVERSE ISOLATION

	GOAL	1	2	3	4	5	6
BUFFER AMPLIFIER	50	49.5	49.2	49.6	50	49.5	50
BROADBAND AMPLIFIER	30	34.8	35	34.8	35	34.4	34.5
73.8 MHZ MEDIUM GAIN AMPLIFIER	70	59	59	59.8	62.5	60.5	63.5
70 MHZ MEDIUM GAIN AMPLIFIER	70	69.5	67.5	69.7	67	69	67.5
IF AMPLIFIER	70	63.5	62.8	63.1	62.5	63.3	62.8

MEASUREMENTS = DB

Table 4. BANDWIDTH

	GOAL	1	2	3	4	5	6
BUFFER AMPLIFIER	20	> 20	> 20	> 20	> 20	> 20	> 20
BROADBAND AMPLIFIER	40	> 40	> 40	> 40	> 40	> 40	> 40
73.8 MHZ MEDIUM GAIN AMPLIFIER	2.0	1.5	1.6	1.6	1.5	1.6	1.6
70 MHZ MEDIUM GAIN AMPLIFIER	10	9.7	10.1	9.5	9.0	9.7	10.2
IF AMPLIFIER	7.0	7.8	7.2	7.9	7.3	6.8	7.7

MEASUREMENTS = MHZ

Table 5. OUTPUT POWER

	GOAL	1	2	3	4	5	6
BUFFER AMPLIFIER	$\geq +10$	$\geq 10$	$\geq 10$	$\geq 10$	$\geq 10$	$\geq 10$	$\geq 10$
BROADBAND AMPLIFIER	$\geq +10$	$\geq 10$	$\geq 10$	$\geq 10$	$\geq 10$	$\geq 10$	$\geq 10$
73.8 MHZ MEDIUM GAIN AMPLIFIER	$\geq +10$	$\geq 10$	$\geq 10$	$\geq 10$	$\geq 10$	$\geq 10$	$\geq 10$
70 MHZ MEDIUM GAIN AMPLIFIER	$\geq +10$	$\geq 10$	$\geq 10$	$\geq 10$	$\geq 10$	$\geq 10$	$\geq 10$
IF AMPLIFIER	$\geq +10$	$\geq 10$	$\geq 10$	$\geq 10$	$\geq 10$	$\geq 10$	$\geq 10$

MEASUREMENTS = DBM

Table 6. VSWR, INPUT AND OUTPUT

	GOAL	1	2	3	4	5	6
BUFFER AMPLIFIER	<2.0:1	<2	<2	<2	<2	<2	<2
BROADBAND AMPLIFIER	<2.0:1	<2	<2	<2	<2	<2	<2
73.8MHZ MEDIUM GAIN AMPLIFIER	<2.0:1	<2	<2	<2	<2	<2	<2
70MHZ MEDIUM GAIN AMPLIFIER	<2.0:1	<2	<2	<2	<2	<2	<2
IF AMPLIFIER	<2.0:1	<2	<2	<2	<2	<2	<2

MEASUREMENTS = ---:1

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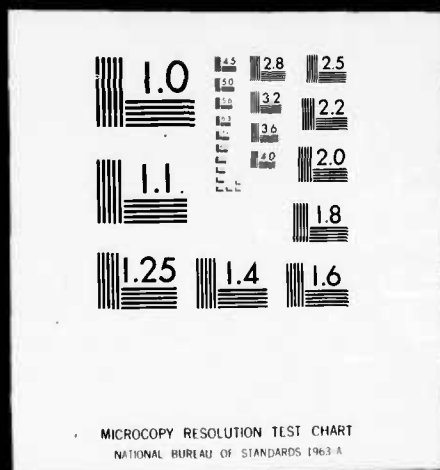


Table 7. INPUT POWER

	1	2	3	4	5	6
BUFFER AMPLIFIER	12	12	12	12	12	12
BROADBAND AMPLIFIER	13.5	13	12.5	11.5	12.5	12
73.8 MHZ MEDIUM GAIN AMPLIFIER	22	21	20	21	21	21
70 MHZ MEDIUM GAIN AMPLIFIER	21	21	20	21	21	20
IF AMPLIFIER	28	27	27	28	28	26

MEASUREMENTS = MA

Table 8. AGC SENSITIVITY and RANGE

IF AMPLIFIER	GOAL	1	2	3	4	5	6
RANGE (DB)	55	55	55	55	55	55	55
SENSITIVITY (V/DB)	.02 <del>10</del> .04	.025	.023	.023	.025	.025	.024
AGC INPUT (VDC)		1.35	1.28	1.25	1.40	1.38	1.35

Table 9. INTERCEPT POINT

	1	2	3	4	5	6
BUFFER AMPLIFIER	+26	+25.5	+26	+25	+25	+25
BROADBAND AMPLIFIER	+16	+16	+16	+16	+15.5	+16
73.8 MHZ MEDIUM GAIN AMPLIFIER	+18	+19	+19	+19	+18.5	+18
70 MHZ MEDIUM GAIN AMPLIFIER	+18.5	+18	+19.5	+18.5	+20	+19
IF AMPLIFIER	+18	+18.5	+20	+18.5	+18.5	+18.5

MEASUREMENTS = DBM

Table 10. NOISE FIGURE

	1	2	3	4	5	6
BUFFER AMPLIFIER	> 20 DB	> 20 DB	> 20 DB	> 20 DB	> 20 DB	> 20 DB
BROADBAND AMPLIFIER	16.4 DB	16.4 DB	16.4 DB	15.6 DB	15.8 DB	15.9 DB
73.8 MHZ MEDIUM GAIN AMPLIFIER	10.5 DB	9.8 DB	9.4 DB	9.9 DB	9.8 DB	10.6 DB
70 MHZ MEDIUM GAIN AMPLIFIER	5.9 DB	6.2 DB	6.7 DB	6.5 DB	6.8 DB	6.8 DB
IF AMPLIFIER	15.9 DB	16.8 DB	17.1 DB	18.2 DB	15.8 DB	18.5 DB

TABLE 11. BANDPASS, 73.8 MHZ MEDIUM GAIN AMPLIFIER

#1			#2			#3			#4			#5			#6		
Freq.	dB	Freq.	Freq.	dB	Freq.	Freq.	dB	Freq.	Freq.	dB	Freq.	Freq.	dB	Freq.	Freq.	dB	Freq.
73.4	-1	74.2	73.3	-1	74.3	73.3	-1	74.4	73.4	-1	74.3	73.3	-1	74.3	73.3	-1	74.3
73.2	-2	74.4	73.2	-2	74.5	73.1	-2	74.5	73.2	-2	74.4	73.1	-2	74.5	73.0	-2	74.4
73.1	-3	74.6	73.1	-3	74.69	73.0	-3	74.7	73.0	-3	74.5	73.0	-3	74.6	72.9	-3	74.5
72.9	-5	74.8	72.8	-5	74.9	72.8	-5	74.9	72.8	-5	74.7	72.8	-5	74.9	72.7	-5	74.8
72.4	-10	75.4	72.4	-10	75.3	72.4	-10	75.3	72.4	-10	75.2	72.4	-10	75.4	72.2	-10	75.3
71.3	-20	76.7	71.4	-20	76.5	71.6	-20	76.3	71.5	-20	76.1	71.4	-20	76.5	71.2	-20	76.4
70.1	-30	78.6	70.4	-30	77.8	70.5	-30	77.7	70.5	-30	77.4	70.3	-30	78.1	70.1	-30	78.1
68.6	-40	82.3	69.1	-40	79.9	69.2	-40	79.5	69.2	-40	79.0	69.0	-40	80.5	68.7	-40	80.6
65.0	-50	89.2	67.5	-50	82.7	67.6	-50	81.9	67.6	-50	80.6	67.5	-50	84.2	67.3	-50	84.9

TABLE 12. BANDPASS, 78 MHZ MEDIUM GAIN AMPLIFIER

#1			#2			#3			#4			#5			#6		
Freq.	dB	Freq.	Freq.	dB	Freq.	Freq.	dB	Freq.	Freq.	dB	Freq.	Freq.	dB	Freq.	Freq.	dB	Freq.
	From Ref.			From Ref.			From Ref.			From Ref.			From Ref.			From Ref.	
66.1	- 1	73.1	66.2	- 1	73.8	66.3	- 1	73.7	66.3	- 1	73.5	66.1	- 1	73.9	65.8	- 1	74.1
65.4	- 2	74.2	65.4	- 2	74.4	65.7	- 2	74.4	66.0	- 2	74.2	65.7	- 2	74.5	65.3	- 2	74.7
65.1	- 3	74.8	74.9	- 3	74.9	65.4	- 3	75.0	65.7	- 3	74.7	65.3	- 3	75.0	65.0	- 3	75.2
64.5	- 5	75.8	64.2	- 5	75.9	64.9	- 5	75.9	65.1	- 5	75.5	64.8	- 5	75.7	64.5	- 5	76.0
63.3	-10	77.7	62.8	-10	77.9	63.5	-10	78.2	64.1	-10	77.3	63.6	-10	77.9	63.3	-10	78.1
61.0	-20	83.4	60.4	-20	84.0	60.7	-20	83.4	61.9	-20	82.4	61.4	-20	83.4	61.1	-20	83.9
58.3	-30	92.7	57.9	-30	93.3	58.1	-30	89.2	59.4	-30	91.2	58.9	-30	90.3	58.7	-30	91.5
55.7	-40	101.7	55.5	-40	101.7	55.7	-40	96.9	56.6	-40	99.7	56.2	-40	98.1	56.3	-40	99.4
53.0	-50	113.3	53.0	-50	113.3	53.1	-50	107.5	53.8	-50	110.4	53.4	-50	108.8	53.7	-50	110.6

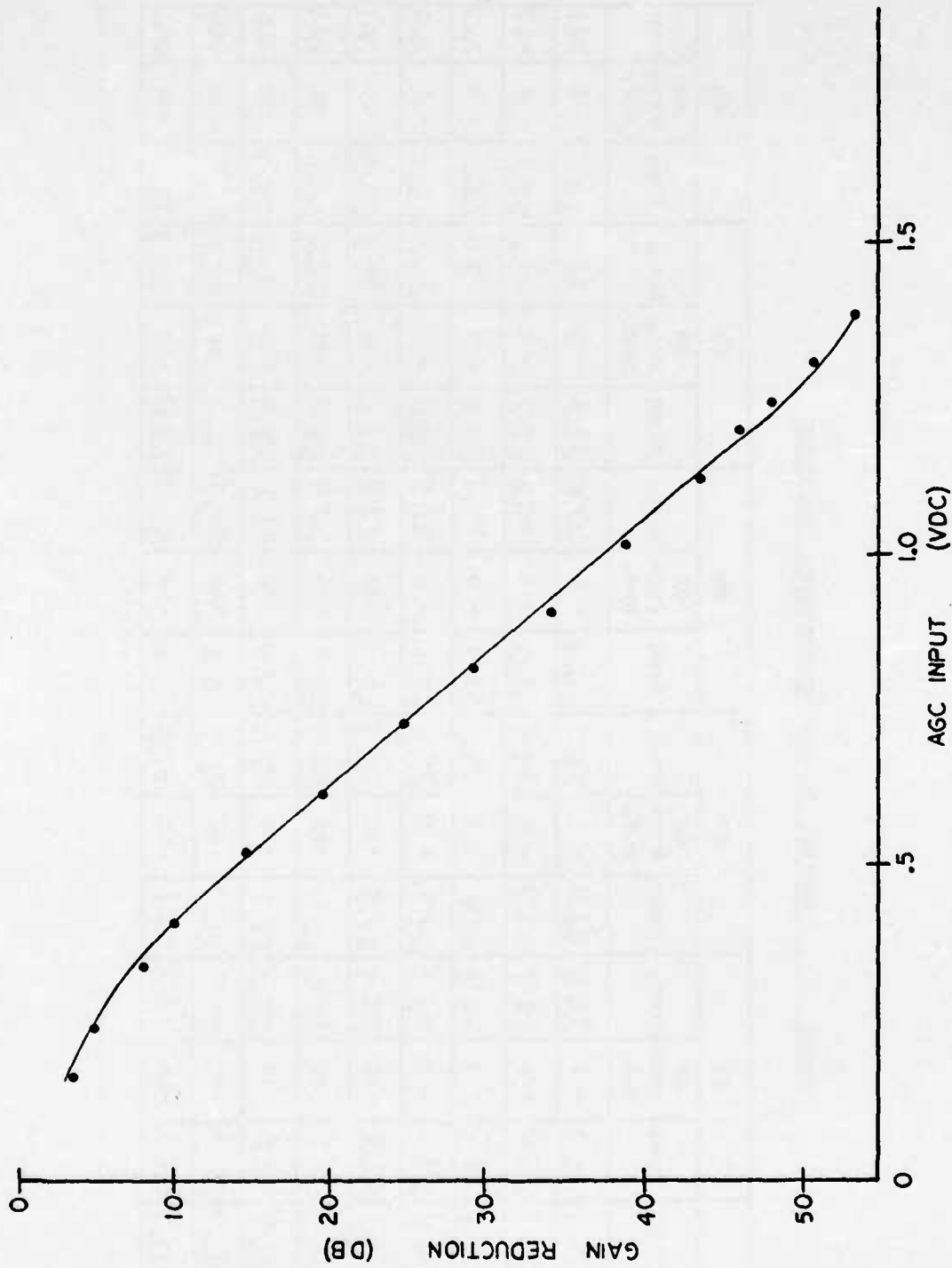


Figure 67. AGC Input vs Gain Reduction, Serial No. 1

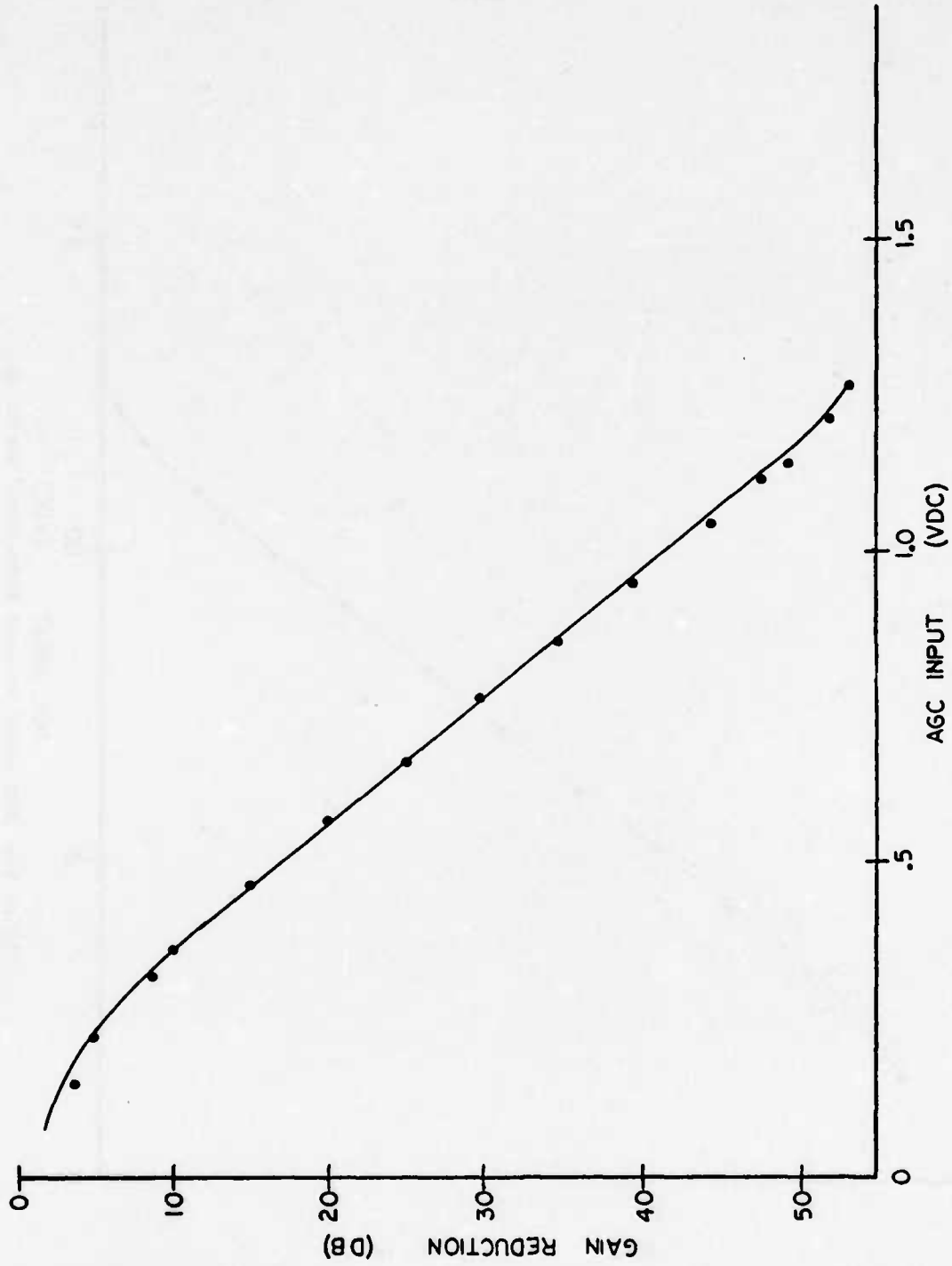


Figure 68. AGC Input vs Gain Reduction, Serial No. 2

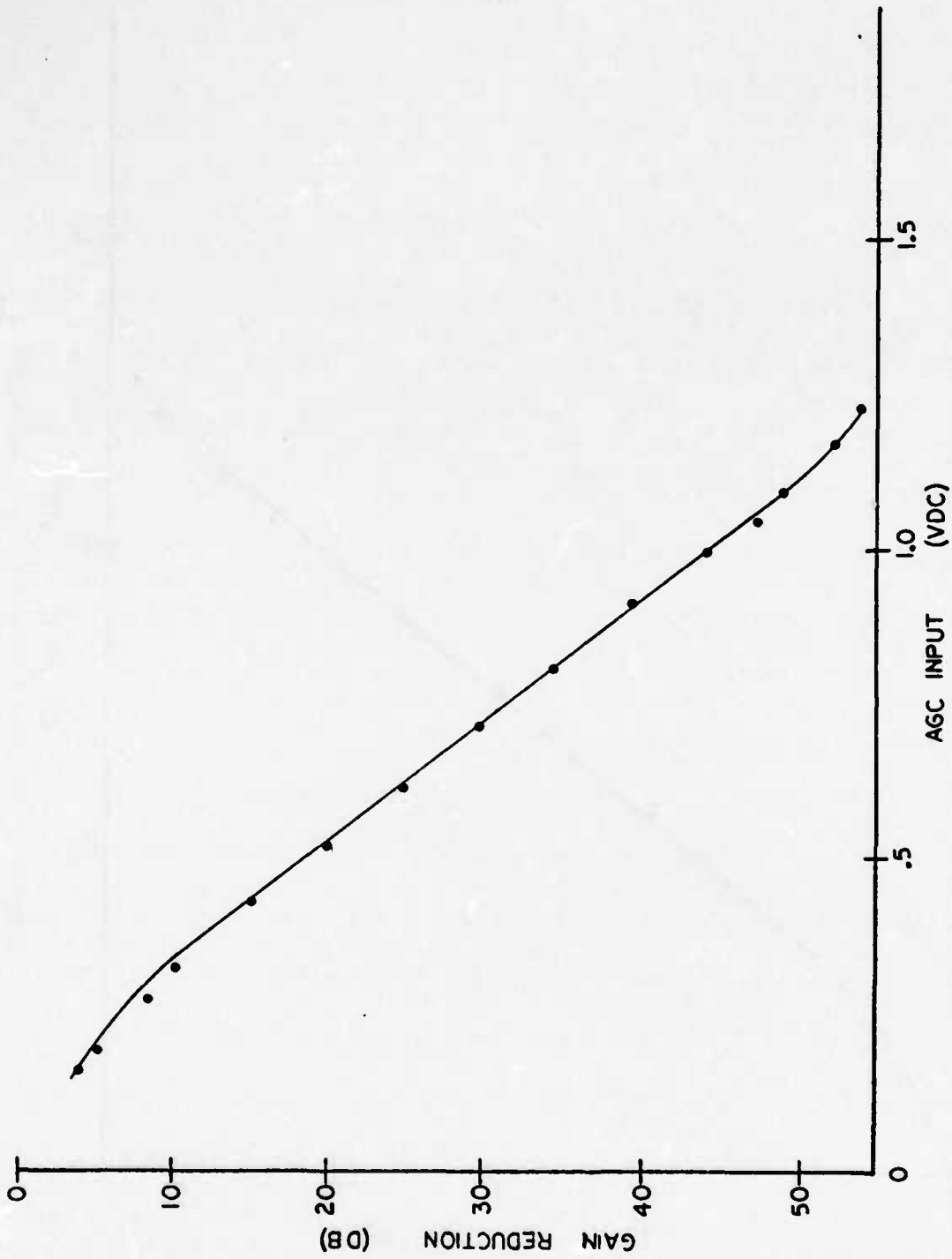


Figure 69. AGC Input vs Gain Reduction, Serial No. 3

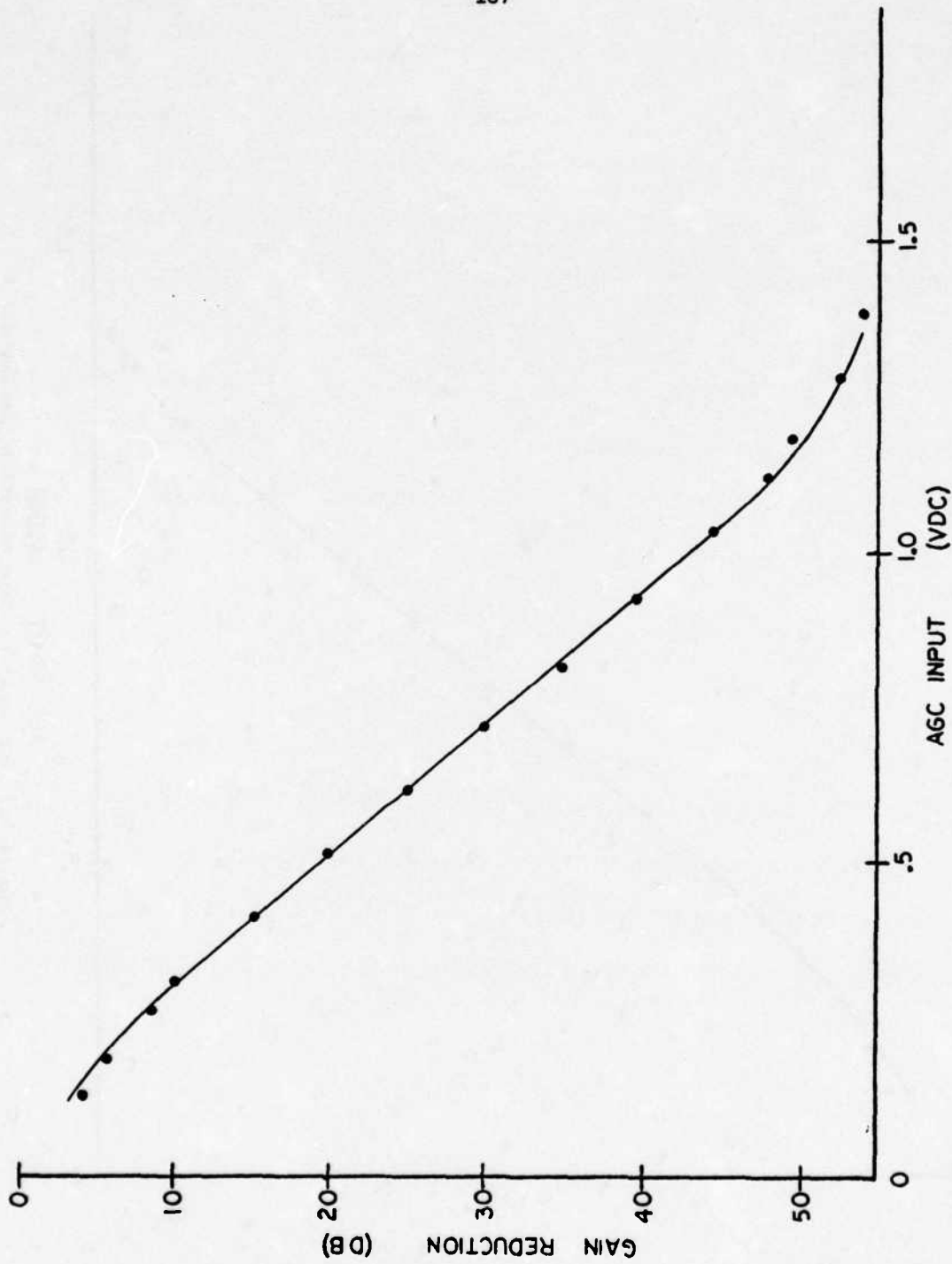


Figure 70. AGC Input vs Gain Reduction, Serial No. 4

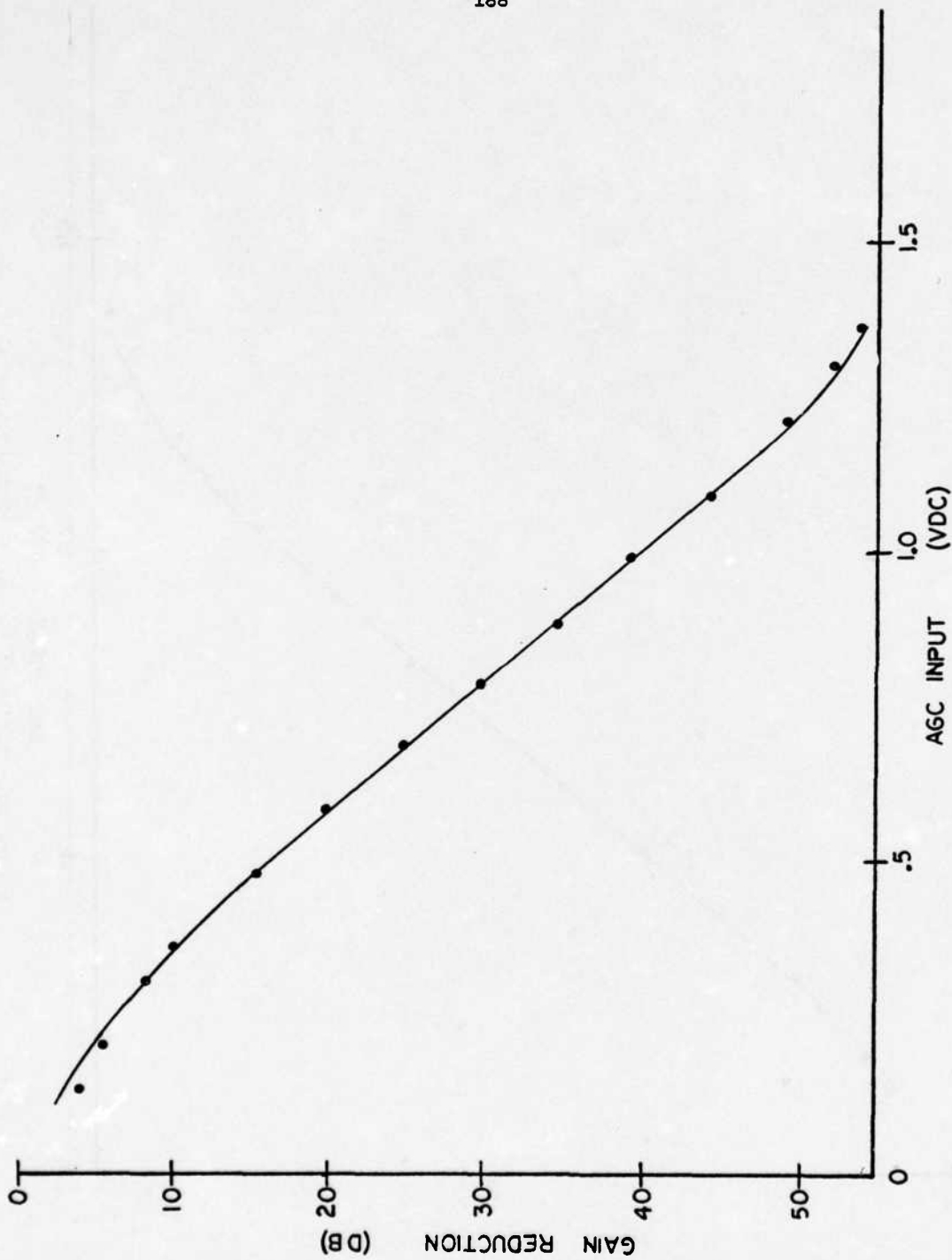


Figure 71. AGC Input vs Gain Reduction, Serial No. 5

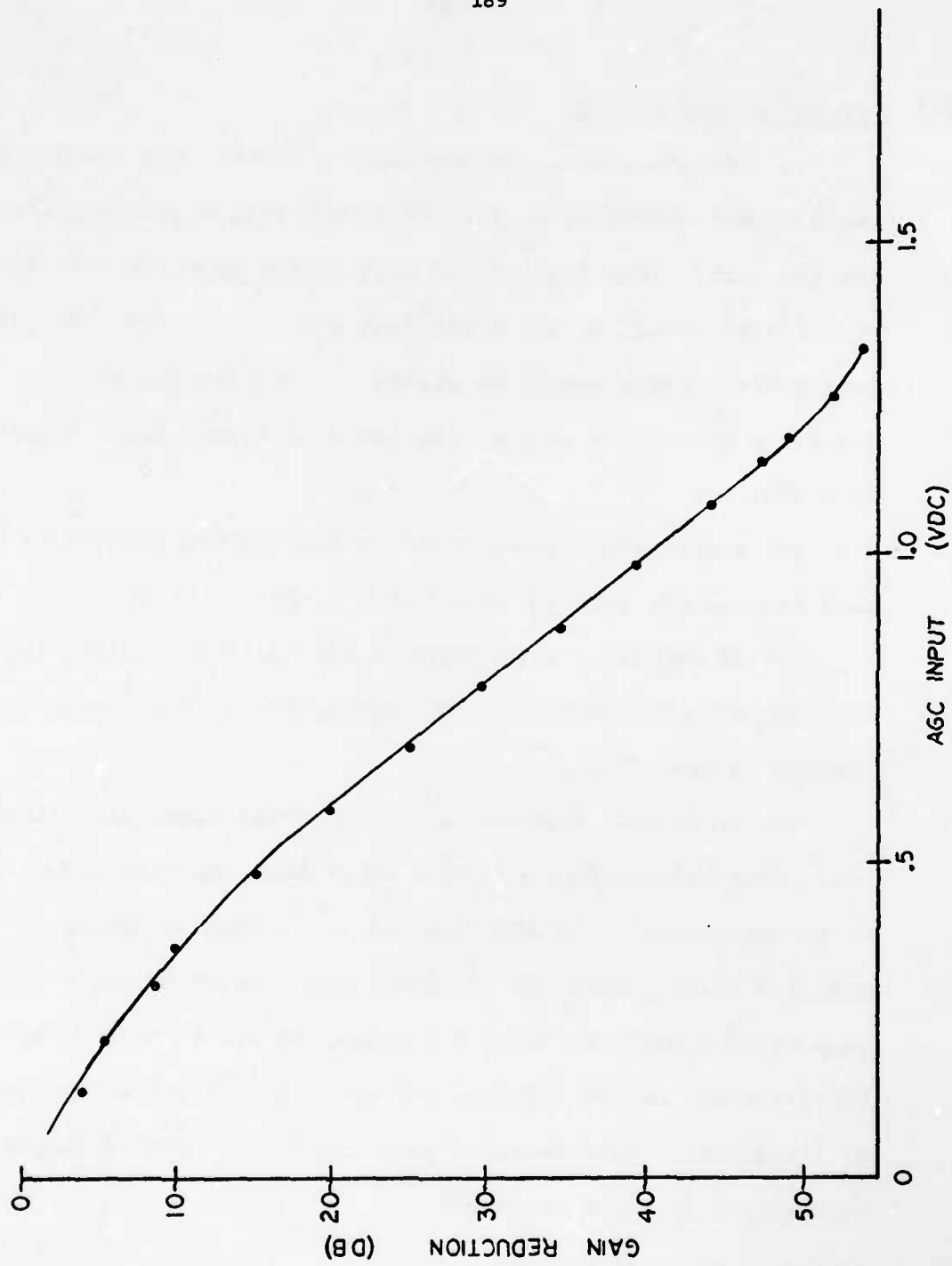


Figure 72. AGC Input vs Gain Reduction, Serial No. 6

### 3.2.5 Operation Instructions

The operating instructions for the buffer, the broadband, the 73.8 MHz medium gain, and the 70 MHz medium gain amplifier are the same. They require the application of a +12 volt supply to the feedthrough on the upper side that is labeled +12V and have current requirements as stated in the previous section, 3.2.4. A ground lug is also available if ground is not otherwise obtained.

The signal input and output are through BNC connectors at each end and are labeled IN and OUT on the top cover.

The IF amplifier also requires +12 volts to the terminal, labeled +12V and the signals are again through BNC connectors, labeled IN and OUT.

One additional terminal is found on the upper side labeled AGC. This allows the input of a DC voltage for gain reduction of the amplifier. The AGC terminal is to operate between 0 and +1.5 volts. Although no damage will result if the voltage goes below 0 volts or above 1.5 volts, as stated before, the amplifier may become unstable and oscillate if the AGC voltage goes negative. This terminal also should not open if proper performance is to be expected.

### 3.2.6 Modification Instructions

To meet the general requirements the amplifiers may be modified to change operating characteristics. Given here are

the changes in gain, bandwidth, and center frequency which may be desirable for each unit, and a procedure to accomplish them.

A) With the Buffer Amplifier it may be desirable to change the gain or the center frequency. To change the gain requires modification of the input attenuator consisting of R5, R6, and R7 of Figure 62, a 20dB symmetrical Pi pad. To change to 10dB gain would require a 10dB pad. The new resistor values are obtained from the 5th edition of the ITT Reference Data Manual, Page 10-6. From Table 2 an attenuation of 10dB requires shunt arms of 962.5 ohms and a series arm of 711.5 ohms for a 500-ohm characteristics system. With a 50-ohm characteristic system it is necessary to divide the resistances by ten. This results in shunt arms of 96.25 ohms and a series arm of 71.15 ohms. The closest standard resistor values are a series arm of 68 ohms and a shunt arm of 100 ohms. The change in characteristic impedance and attenuation from moving the resistors to the nearest standard value in this case is insignificant.

For illustrations on how to change the operating frequency of the amplifier stage, a center frequency of 60 MHz is selected. The first step is to obtain the Y-parameters at 60 MHz from a manufacturer's data sheet on the 2N918 transistors. They are:

$$Y_{11} = 3 + j3.5 \text{ mmhos}$$

$$Y_{12} = -j.4 \text{ mmhos}$$

$$Y_{21} = 52 - j35 \text{ mmhos}$$

$$Y_{22} = .3 + j.9 \text{ mmhos}$$

The stability of the transistor is then checked using the Linvill stability factor of:

$$C = \frac{|Y_{12} Y_{21}|}{2g_{11} g_{22} - \text{Re}(Y_{12} Y_{21})} = \frac{25.08}{1.8 + 13.99} = 1.58$$

A factor greater than one indicates the transistor is potentially unstable. This condition was also encountered at 70 MHz and was compensated by including a 1000 ohm resistor in the collector circuit. For simplicity the 1000-ohm resistor will also be used here.

The next step is to determine the collector circuitry to resonate at 60 MHz, and also a matching network to transform the transistor output impedance to 50 ohms. Using the following diagram:

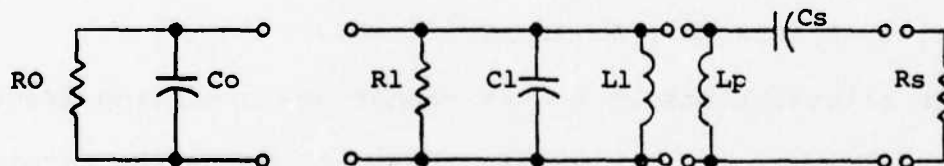


Figure 73. Collector Circuitry and Matching Network

The first section represents the transistor output and is obtained from  $Y_{22} = .3 + j.9 \text{ mmhos}$ , as:

$$R_O = \frac{1}{.3 \text{ mmhos}} = 3333 \text{ ohms and } C_O = \frac{.9 \text{ mmhos}}{\omega} = 2.4 \text{ pf}$$

where  $\omega = 2\pi f$  with  $f = 60 \text{ MHz}$ .

The second section is the fixed components of the collector tank circuit consisting of  $R_1 = 1000 \text{ ohms}$ , and  $C_1$  and  $L_1$  to be determined later. The third section is an L-section matching network to transform  $R_p$  to  $R_s = 50 \text{ ohms}$ .  $R_p$  is the parallel equivalent resistance of  $R_0$ ,  $R_1$ , and the parallel resistance of  $L_1$ . The parallel resistance of the inductor is normally large compared to  $R_0$  and  $R_1$ , and is neglected. The equations for the matching network are:

$$\frac{R_p}{R_s} = Q^2 + 1, \quad X_p = \frac{R_p}{Q} \quad \text{and} \quad X_s = R_s Q$$

with  $R_p = 769 \text{ ohms}$  then  $Q = 3.79$ ,  $X_p = 203 \text{ ohms}$ , and

$X_s = 189 \text{ ohms}$ . The value of  $C_s$  is found from

$$C_s = \frac{1}{\omega X_s}$$

to be approximately 14 pf. The closest standard value for  $C_s$  is 15 pf.  $L_p$  is found from

$$L_p = X/\omega$$

and is equal to  $.54 \mu \text{ h}$ .

The fixed capacitor  $C_1$  is selected at 10 pf, a value large enough to control tuning variations caused by transistor parameter changes on  $C_0$ , yet small enough to avoid an unobtainable value of inductance to resonate the tank circuit.

$L_1$  is the inductance required to resonate with  $C_1$  and  $C_0$ , and

from

$$L_1 = \frac{1}{\omega^2 (C_0 + C_1)}$$

$L_1$  is equal to  $.57\mu\text{h}$ . Since the actual circuit has only one inductor it will be the parallel equivalent of  $L_1$  and  $L_p$ . The closest standard value of inductance for the combination is  $L_{eq} = .27\mu\text{h}$ . The component values for  $R_1$ ,  $C_1$ ,  $C_s$  and  $L_{eq}$  in Figure 6 are then used for  $R_4$ ,  $C_4$ ,  $C_6$ , and  $L_2$  in Figure 1.

The next step is to determine the input circuit as shown in Figure 74:

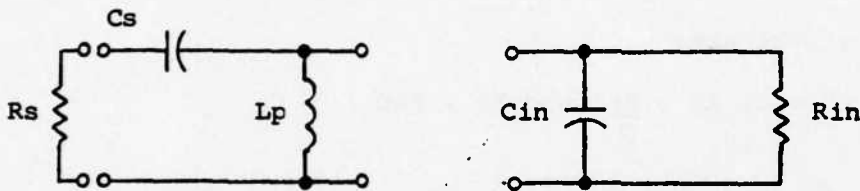


Figure 74. Input Circuit

$R_{in}$  and  $C_{in}$  represent the input admittance and are found from

$$Y_{in} = Y_{11} - \left( \frac{Y_{12} Y_{21}}{Y_{22} + Y_L} \right)$$

where  $Y_L$  is the load admittance of the output circuit consisting of  $R_1$ ,  $C_1$ ,  $L_1$ ,  $L_p$ ,  $C_s$  and  $R_s$ . For  $Y_L = 1.48 - j.8 \text{ mmhos}$  the input admittance is  $11.49 + j14.72 \text{ mmhos}$ . This results in

$$R_{in} = \frac{1}{11.49 \text{ mmhos}} = 87 \text{ ohms, and}$$

$$C_{in} = \frac{14.72 \text{ mmhos}}{\omega} = 39 \text{ pf}$$

The values for  $C_s$  and  $L_p$  of Figure 74 are found by using the equations for a matching network. From the equations  $Q = .86$ ,  $X_p = 101$ , and  $X_s = 43$  for  $R_p = R_{in}$ . Using the value for  $X_s$ ,  $C_s$  is found to be 61 pf. The next standard value is 68 pf.  $L_p$  is the equivalent of the matching network inductance

and the inductance needed to resonate with  $C_{in}$ . The two inductances are found from

$$\frac{X_p}{\omega} = \frac{R}{\omega} \frac{p/Q}{\omega}, \text{ and } \frac{1}{\omega^2 C_{in}}$$

to be  $.26\mu h$  and  $.18\mu h$ .

The equivalent inductance is  $L_p = .106\mu h$  with  $.1\mu h$  being the closest standard value. The component values of  $C_s$  and  $L_p$  in Figure 74 represent  $C_1$  and  $L_1$  in Figure 62.

After calculating the source admittance of  $Y_s = 12.44 + j9.69\text{mmhos}$  the circuit stability may be found from the stability factor described by Stern. The stability factor is:

$$k = \frac{2(G_s + g_{11})(G_L + g_{22})}{|Y_{12}Y_{21}| + R_e(Y_{12}Y_{21})}$$

where  $G_s$  and  $G_L$  are the real part of  $Y_s$  and  $Y_L$ . If  $k$  is greater than one the circuit will be stable, and if  $k$  is less than one the circuit will be unstable. From the parameter values given previously,

$$k = \frac{2(12.44+3)(1.48+.3)}{25.08-13.99} = 4.95$$

which is greater than one, therefore, the circuit will be stable.

The predicted gain is calculated from

$$G_t = \frac{4 R_e(Y_s) R_e(Y_L) |Y_{21}|^2}{|(Y_{11}+Y_s)(Y_{22}+Y_L)-Y_{12}Y_{21}|^2} \quad \text{and}$$

is found to be approximately 79.5, which is equivalent to 19dB.

Since the component values were obtained from calculations and the calculations contain approximations, it may be necessary to alter some values experimentally to obtain a precise circuit performance. It should also be noted that, although this discussion established the output circuitry first, an equivalent result would be obtained by determining the input circuitry and then conjugate matching the output.

B) The Broadband Amplifier has a 40 MHz bandwidth and already offers a wide range of operating frequencies. Therefore, a change of gain would probably be the only desirable change. This amplifier is preceded by a 6dB attenuator and has a 10dB gain. Therefore, its gain may be decreased 10dB or increased 6dB by changing the attenuator as indicated in the previous section.

C) The 73.8 Medium Gain Amplifier was designed for a specific use and would, therefore, not be desirable to change. It does have a 4dB pad consisting of R5, R6, R7 (Figure 64) which may be modified as previously indicated to provide any desired gain from 0dB to 34dB.

D) The 70 MHz Medium Gain Amplifier contains two amplifier stages whose operating frequency could be changed as illustrated in Section 3.2.6 (A). It also has a 9dB attenuator consisting of R5, R6, and R7 (Figure 65) that may be changed for 0dB to 39dB of gain, as illustrated in the same section.

This unit also contains a three-pole filter that may be changed to alter the bandwidth. To illustrate a change of bandwidth the present bandwidth of 10 MHz at a 70 MHz center frequency will be changed to a 2 MHz bandwidth at the 70 MHz center frequency.

If the same inductors are used that have a  $Q$  of 120 and are approximately  $.1\mu\text{H}$ , then a predicted insertion loss from Page 8-39, Figure 47 of the ITT Handbook is about 8dB. This figure is for a three-pole filter with a normalized  $q = Q_0/\text{Fo}/\text{BW} = 120/7/2 = 3.43$ . Using  $q = 3.43$  from Page 8-37, Figure 44 of the ITT Handbook the predistorted  $k$  and  $q$  values can be obtained. These are used because it is a small percentage band-pass circuit. From the graph,  $q_1 = .86$ ,  $q_2 = 1.8$ ,  $k_{12} = .55$  and  $k_{23} = .74$ . Using the equations given with Figure 28A, Page 8-25 of the ITT Handbook, component values for the circuit shown in Figure 75 may be found.

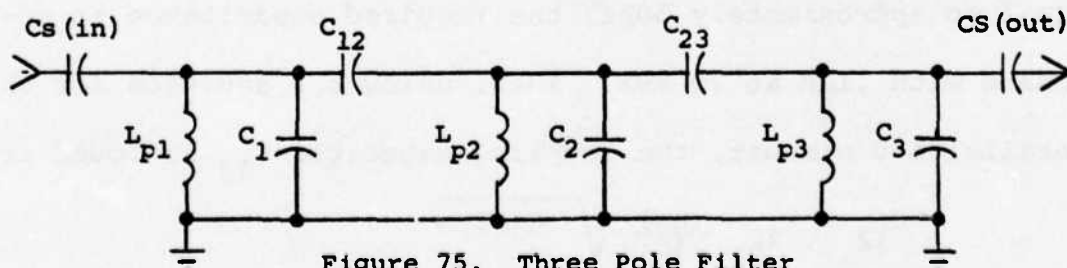


Figure 75. Three Pole Filter

The  $Q$  of the end resonators are calculated as follows:

$$Q_1 = q_1 (f_0/\text{BW}) = .86 \frac{(70)}{2} = 30.1 \quad \text{and}$$

$$Q_3 = q_3 (f_0/\text{BW}) = 1.8 \frac{(70)}{2} = 63$$

The parallel inductors are already .1 microhenries which have a parallel reactance of approximately 50 ohms. With  $X_p=50$  ohms and  $Q_1 = 30.1$ , then  $R_{p1} = X_p Q_1 = 1505 \Omega$ . To use this filter in a 50-ohm system requires matching 1505 ohms down to 50 ohms. The transformation is done through a series capacitance, where

$$X_{cs} = R_s Q, \text{ and } Q = \sqrt{\frac{R_p}{R_s} - 1}.$$

Substitution gives

$$Q = \sqrt{\frac{1505}{50} - 1} = 5.39 \text{ and } X_{cs} = 50(5.39) = 269.5 ; \text{ from this,}$$

$$C_s (\text{in}) = \frac{1}{2\pi f_o X_c} = 8.4 \text{ pf.}$$

For the third resonator a similar calculation using  $Q_3 = 63$  gives  $R_{p3} = 3150$  ohms,  $Q = 7.87$ , and  $X_c = 3.93.7$ . From this  $C_s (\text{out}) = 5.8\text{pf}$  is obtained. Referring back to Figure 75 the parallel capacitance  $C_1$  and  $C_2$  will be assumed equivalent and equal to approximately 50pf; the required capacitance to resonate with .1 $\mu\text{H}$  at 70 MHz. Then, using the equation for the parallel L-C circuit, the coupling capacitor  $C_{12}$  is found from

$$C_{12} = k_{12} \frac{(BW)}{f_o} \sqrt{C_1 C_2}$$

Using  $k_{12} = .55$  and  $C_1 = C_2 = 50\text{pf}$ ,  $C_{12} = .78 \text{ pf.}$

The other coupling capacitor  $C_{23}$  is

$$C_{23} = k_{23} \frac{(BW)}{f_o} \sqrt{C_1 C_2}$$

where  $k_{23} = .74$  and results in  $C_{23} = 1.04 \text{ pf.}$

$C_{12}$  and  $C_{23}$  are represented by C9 and C12 in Figure 65. Obtainable capacitors near the calculated values are .5, 1.0, and 1.5pf. Of these, both C9 and C12 are closest to 1.0pf. As these are calculated values and assumptions have been made, it may be necessary to increase or decrease either one or both capacitors to the next standard value to obtain the desired bandwidth.  $C_s$  (out) is equivalent to C15 in Figure 65, and a 6 pf capacitor would be the closest standard value for this component. Again, it may be necessary to alter this value if proper tuning of the filter does not result.  $C_s$  (in) = 8.4pf is the value necessary to match the filter to 50 ohms, but in the actual circuit C6 matches the output of Q1 to the filter. An 18pf capacitor is needed to match the output of Q1 to 50 ohms, as can be seen of C21 in Figure 65; therefore, C6 is the series combination of 18pf and 8.4pf. This results in  $C6 = 5.7\text{pf}$  with the closest standard value being 6pf. This may also need some adjustment if the proper tuning is not obtained. With  $L3 = L4 = L5 = .1\mu\text{h}$  and requiring approximately 50pf to resonate them, making the calculated changes to C6, C9, C12 and C15 the amplifier should tune at 70 MHz with a 2 MHz bandwidth without altering the other components. However, C7 and C13 may need to be changed from 22pf to 27pf if the filter tunes to a frequency higher than 70 MHz.

As was indicated the insertion loss is greater with the smaller bandwidth and consequently the overall gain will be less. To maintain the same gain the attenuator network of R5, R6, and R7 can be changed.

E) The IF Amplifier has a variable gain so that the bandwidth and operating frequency would be the only desirable changes, and bandwidth changes would be inappropriate since no filter is available. A change in operating frequency of the MC15906 would follow a y-parameter design approach similar to the one covered previously. The y-parameters are obtained from the manufacturer's data then the procedure outlined in Section 3.2.6 (A) can be followed. It would also be necessary to change the output stage by the same method.

### 3.3 CONCLUSIONS

In the building of the 70 MHz amplifiers some areas for consideration when designing amplifiers of this type have been noted.

When trying to obtain a large reverse isolation the goal can be affected by transistor parameters. In the design of a single-stage amplifier the reverse isolation was found to be inversely related to  $C_{ob}$ , the collector-to-base capacitance. A reverse isolation of 30dB could be expected if the  $C_{ob}$  was no greater than one picofarad, but as the capacitance increased the reverse isolation decreased. Since the capacitance is fixed as a result of the manufacturing process, and varies from

transistor to transistor, this becomes a limiting factor as to the isolation that can be expected. Reverse isolation can also be affected by physical size. When the signal levels become high and the distance from the input to output gets short enough, sufficient cross coupling can occur to reduce the isolation.

Obtaining narrow filters with bandwidths in the area of 5% or less of center frequency can also pose some difficulties when trying to maintain a minimum package size. Discrete component values begin to be impractical; since, only very light coupling is required between filter resonators the stray capacitances may be greater than the actual component. With narrow bandwidths the resonator  $Q$  must be high and cross coupling between resonators begins to affect the frequency response. It is then necessary to separate the resonators by shielding, or physically separating them if possible. If the bandwidth is much less than 5% of center frequency this does not apply since other means of filtering are available. The cross coupling, due to radiation, also has the effect of reducing reverse isolation.

SECTION IV  
SYNTHESIZER

4.1 GENERAL CASE

This section provides information on the general requirements and the design work done to meet the specific requirements for the frequency synthesizer. This synthesizer is required to produce approximately 16 million frequencies with narrow channel spacing over a modest range of frequencies at the low end of the VHF band. The synthesizer has a capability for rapid frequency hopping to any channel desired. Control of the frequencies are to be done digitally with TTL command signals. The output of the synthesizer is sufficient to drive a balanced mixer or frequency multiplier.

The function of the synthesizer is to provide a series of signals. These signals are usually coherent with a reference or clock time base and are proportional to  $f_o = \frac{M}{N} f_{ref}$ . There are three general methods for producing the required frequencies. One approach is the mix/divide synthesizer. The output is generated by taking one or more input signals and by suitable mixing and dividing, an output is generated at the desired frequency. Another approach is to use a VCO and programmable divider chain. The output of the divider chain is phase compared to a reference frequency and used to control the VCO frequency. Changing the programming alters the VCO frequency.

The third approach uses a comb generator to generate a spectrum of frequencies at the desired channel spacing. A VCO and PLL is then used to pick out the desired frequency with the VCO output being the desired signal source. In essence, the PLL forms a tunable filter at the desired harmonic frequency.

#### 4.1.1 Synthesizer Methods and Implementations

The most common approach for generating a stable signal is to employ a phase lock loop which is synchronized to a reference frequency by the action of the loop. The reference frequency frequently is divided down to a lower frequency which is a function of the required channel spacing. At the same time the desired output is generated by a VCO which is also divided down to the reference frequency by means of a programmable divider. Frequency control is provided by changing the frequency of the VCO and the programmed division ratio. The two divided signals are applied to a phase detector from which a control voltage is derived, filtered, and fed to the VCO as a correction voltage. Loop bandwidth is dictated by several requirements, one of which is the reference frequency supplied to the phase detector. The resulting output is related to the input by  $f_{out} = \frac{M}{N} f_{ref}$  where  $N$  is the reference division ratio and  $M$  is the division ratio of the programmable divider. Most synthesizers use this method of frequency synthesis.

The next approach to produce a series of frequencies is also a phase lock loop approach; however, the use of dividers is not necessarily required except to control channel spacing by division of the reference. The method involves the generation of a comb spectrum by the reference source. This comb is used to produce spectral lines at the desired frequencies. A phase lock loop is then used as a narrowband filter to select the desired frequency. The comb becomes the reference input to the phase

detector and the VCO the other input. The output frequency is related to the reference by the following:

$$f_{out} = \frac{M}{N} f_{ref}$$

where  $N$  is the divided reference if division is needed and  $M$  is the desired harmonic line in the comb spectrum. Design parameters for this system are not too unlike those for the synthesizer previously described.

A third method of synthesizing frequencies is to use mix/divide techniques to generate the required signals. This method involves the use of several frequencies mixed together, filtered, divided and filtered again. For example, if ten frequencies at 1MHz spacing are switched to a mixer on command and the resulting output is divided by ten and then mixed back to the original frequency with the same ten switchable frequencies, the result will be 100 generated frequencies in increments of 100KHz (1MHz  $\div$  10). Cascading of the circuit cards will control the channel spacings. Also, the division ratio used on each card can be used to control the channel spacing or both methods can be used simultaneously to control spacing.

All of the previous types of synthesizers have their advantages, disadvantages and limitations. Some of these can be overcome in the design process or may not be a liability depending on system design requirements.

#### 4.1.2 Advantages and Limitations

System requirements will determine the type of synthesizer to be used. One major disadvantage of the PLL synthesizer is that of the capability of providing narrow channel spacing. The phase detector in this type synthesizer has noise components which appear as noise sidebands in the output of the VCO since the phase detector drives the VCO through the loop filter. In order to provide some filtering to the noise components, it is desirable to have the loop bandwidth narrower than the reference frequency to provide filtering. Forty dB of filtering can be provided if the loop bandwidth is 100 times narrower than the reference frequency. Unfortunately, if the channel spacing is narrow the loop design becomes a problem. The VCO may have excessive noise which could keep the loop from staying in lock or the response time may be too long to meet system requirements. This problem does not exist with the mix/divide approach to synthesis. The comb generator type of synthesis is a satisfactory method of generating signals provided the comb spacing is not so narrow as to require a loop bandwidth smaller than 1% of the VCO center frequency. This statement is based on VCO stability considerations. If the loop is narrower than 1% the VCO could drift that much and cause a failure to lock up properly. If oscillator stability is better than 1% the rule can be modified. This problem does not occur in the divider type synthesizer.

The big problem with mix/divide synthesizers is in the large number of spurious responses that are generated in the mixing process. An ideal mixer would produce the product of the two input frequencies and the resultant output would contain only the easily filtered sum and difference frequencies. Unfortunately, the mixer distorts the drive signal producing a complex spectrum. This is also true in relation to the signal to be translated. The result then is a complex spectrum  $M_{f_{lo}} \pm N_{f_{rf}}$ , which in many cases will produce a spectral component that falls into the particular band of interest. This makes the mix/divide type synthesizer an extremely difficult one to build in order to keep undesired signal levels down. Several other problems exist with this type synthesizer depending on spectral purity requirements. An example is that of local oscillator rejection. A local oscillator power level may be required between +10 and +20dBm and if spurious responses are required to be -100dbc, then the level of isolation of the local oscillator to the output needs to be 20dB +100dB or over 120dB for adequate performance. If the output level is lowered for any reason, then the problem becomes even greater. This type of problem does not necessarily exist with the PLL synthesizer and it is possible to provide reasonable isolation to any possible spurious signal sources which do exist within the PLL. This is not true with the mix/divide synthesizer since most of the spurious responses are coming directly out of the mixer ports.

The PLL synthesizer also is difficult to modify for different channel spacings or number of channels. This is not true of the mix/divide synthesizer. The spacings can be modified by supplying different reference frequencies and due to the use of one basic circuit module, the number of channels can easily be changed by increasing or decreasing the number of modules. Another area that the mix/divide approach excels is in settling time. For this type of synthesizer the settling time is limited by the bandwidths of the various filters used and by switch response time. For the PLL it is limited by loop bandwidth and as the channel spacing is reduced to increase the number of channels, the allowable loop bandwidth is reduced and the settling time becomes longer in direct proportion. For the requirement of extremely narrow channels and fast response time, the mix/divide synthesizer is the only choice.

#### 4.1.3 Block Diagrams

A block diagram of a mix/divide synthesizer module is shown in Figure 76. Basically, one of four frequencies are switch selected and used for a local oscillator drive to a mixer. The other mixer input is the lowest switched frequency divided by three. The sum frequency of the mixer is filtered, limited, and divided by four. Since digital circuits are used for the division process, the signal is again filtered and the resultant signal is a pure sine wave at a frequency of  $F + n \frac{\Delta f}{4}$ . This signal is then

fed to the next circuit where the process is repeated. The synthesizer basically consists of a cascade of identical modules all operating in the fashion described. The final module does not necessarily divide the output frequency and for this synthesizer the divider is not used. The final frequency then becomes

$$f_o = 4f + \sum_{i=4}^{12} \frac{n_i \Delta f}{4(i-1)} \quad n = 0,1,2,3$$

with the range of  $i$  a function of the number of circuit boards used in the synthesizer. It can be seen that the final output frequency is at the sum frequency of the mixer. This frequency is buffered, filtered, and amplified to the desired level. A large quantity of shielding is needed to meet the spurious response specifications.

#### 4.1.4 Recommendations

With the requirement for fast response and multiple channels being a necessity, the use of a PLL synthesizer of any type is ruled out, particularly when the need for narrow channel spacing is considered. This means that the only suitable choice is a synthesizer of the mix/divide type. This has inherent disadvantages as previously discussed relating to isolation and signal rejection requirements. The mix/divide synthesizer does have the necessary speed and channelization capabilities. With the choice of a mix/divide synthesizer care will need to be exercised in component selection, circuit layout, and shielding with special techniques used to reduce radiation and crosstalk.

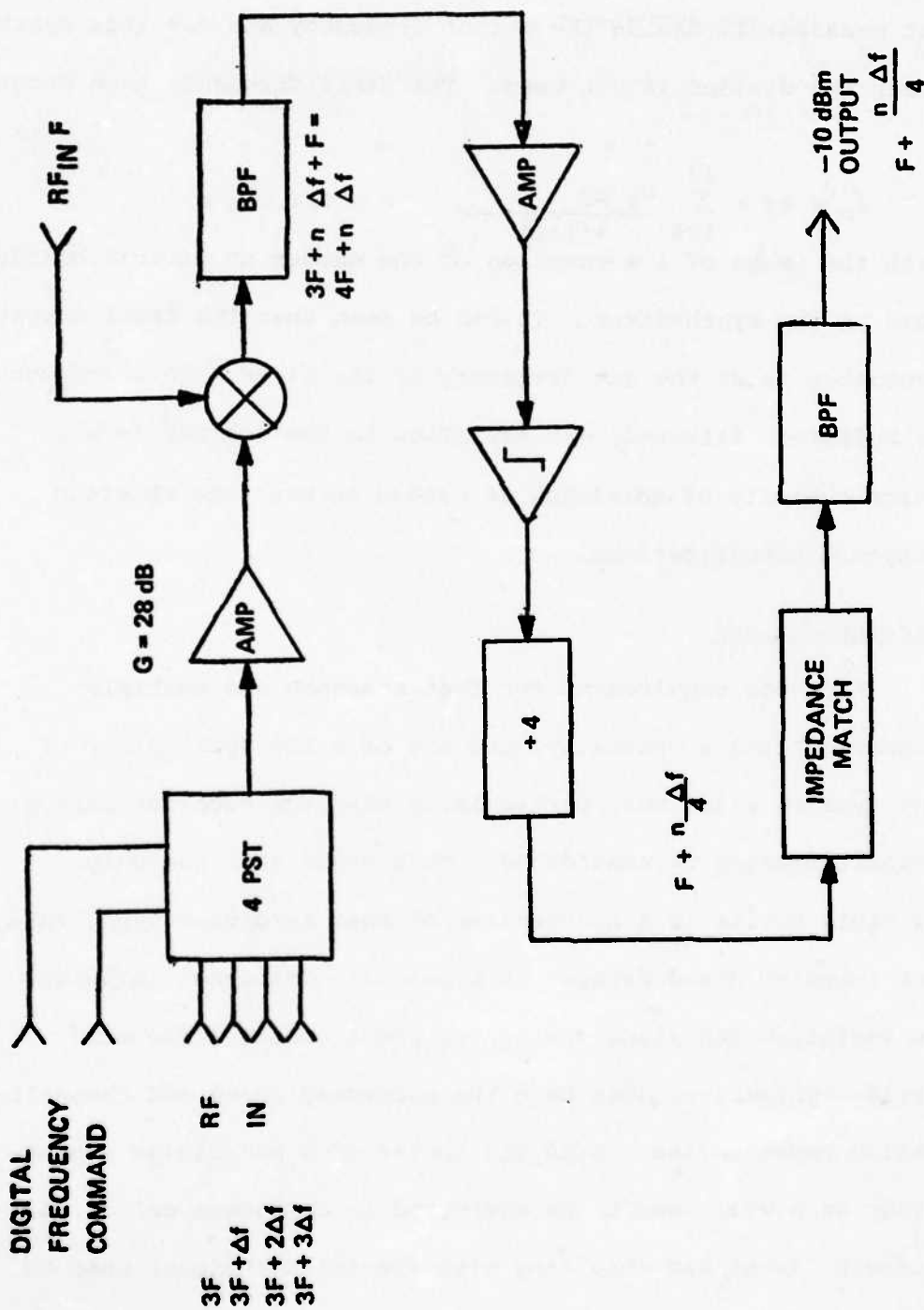


Figure 76. Synthesizer Mix/Divide, Block Diagram

#### 4.2 SPECIFIC CASE

The general requirements were further defined to delineate specific requirements. These specific requirements establish a synthesizer with a known number of channels and a particular channel spacing. The resultant synthesizer is essentially a cascade of identical stages which produce the required results.

##### 4.2.1 Specifications and Requirements

The specific requirements for the synthesizer call for over a million channels with a very narrow channel spacing of less than 1 Hz. The center frequency is in the 400 MHz region. With the channels needed and with the required spacing, the frequencies occupy a band approximately 7 MHz wide. Each mix/divide board provides two bits of the required binary number. The specification calls for all spurious responses to be down at least 100 dbc. Spectral purity will essentially be determined by the quality of signals available from the reference generator. The required settling time will be 100 microseconds with actual response time a good deal faster.

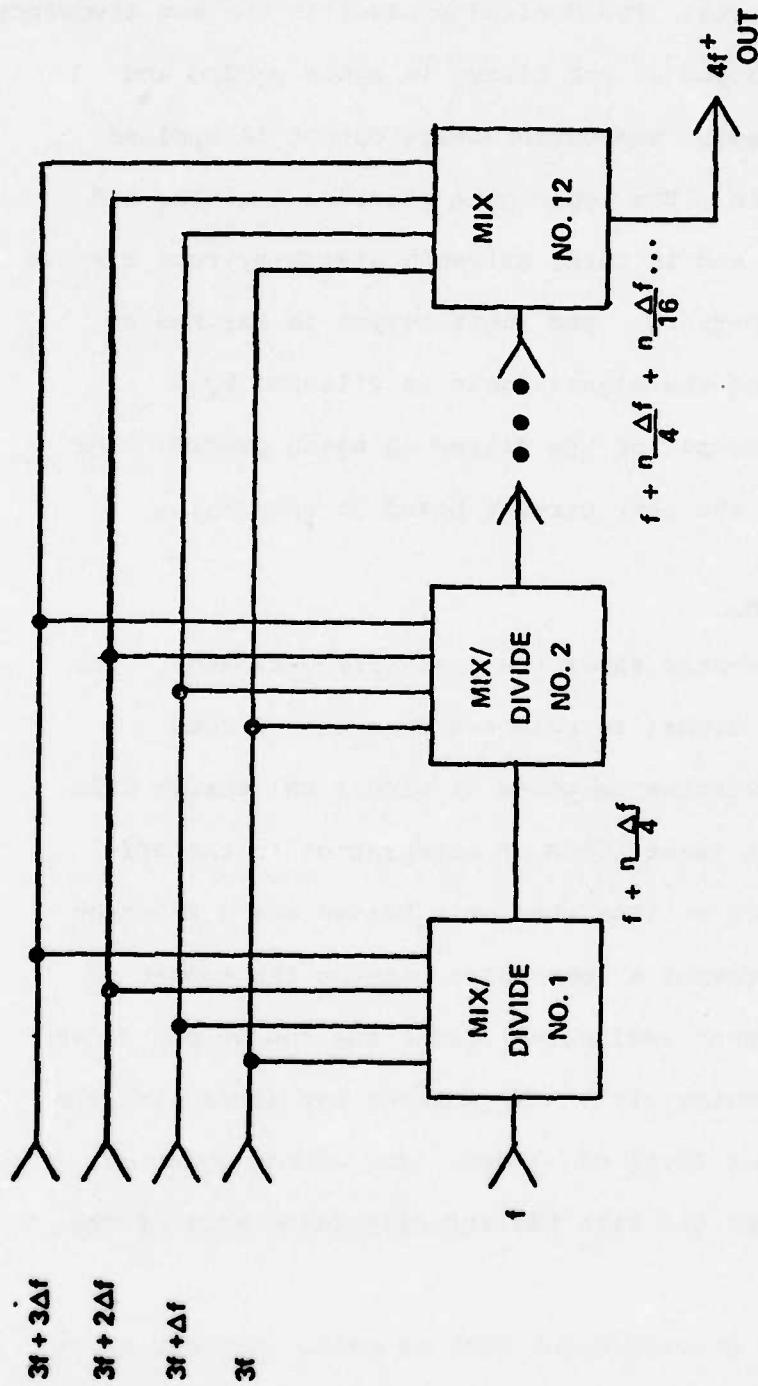
##### 4.2.2 Scheme Used

Figure 76 shown previously, is the general block diagram of a typical mix/divide module. This block diagram applies to eleven of the twelve modules used in the synthesizer. The twelfth module differs in that there is no divider circuit on the card and the output bandpass filter is missing. The synthesizer itself basically consists of a cascaded set of cards with the twelfth card driving a buffer amplifier. The buffer amplifier contains sufficient gain

to provide the required output level to drive any external circuits. The buffer amplifier also has an integral bandpass filter to provide rejection of out-of-band mixer products. Figure 77 shows the chassis block diagram. Each signal applied to J1 through J4 is distributed to each circuit board by means of a twelve-way power splitter. J5 provides an input to the first board directly to the mixer. P1 is the frequency command and power connector for the synthesizer. A TTL compatible 24-bit binary word commands the frequency with all zeros representing the lowest frequency.

The mix/divide board block diagram follows the one originally proposed<sup>1</sup> very closely. Four frequencies are supplied to a diode switch. Each switch output is paralleled and the combination is controlled such that a 4 PST switch is formed. The common output of the switch feeds a two-stage amplifier composed of two 2N918 stages in cascade. This is to boost the RF power level up to a level of at least +13dBm which is the minimum required drive level for the high power mixers used on each mix/divide card. The other input to the mixer is from the preceding card. In the case of the first mix/divide card, the mixer input to the RF port is from an external signal source. The resulting beat note is taken from the IF port of the mixer.

1. Technical Proposal, "Analog Generator and Buffer Circuits, Attachment A Frequency Synthesizer", N-40036 Electronic Communications, Inc.



NOTE: NO. 12 DOES NOT  
HAVE A DIVIDER

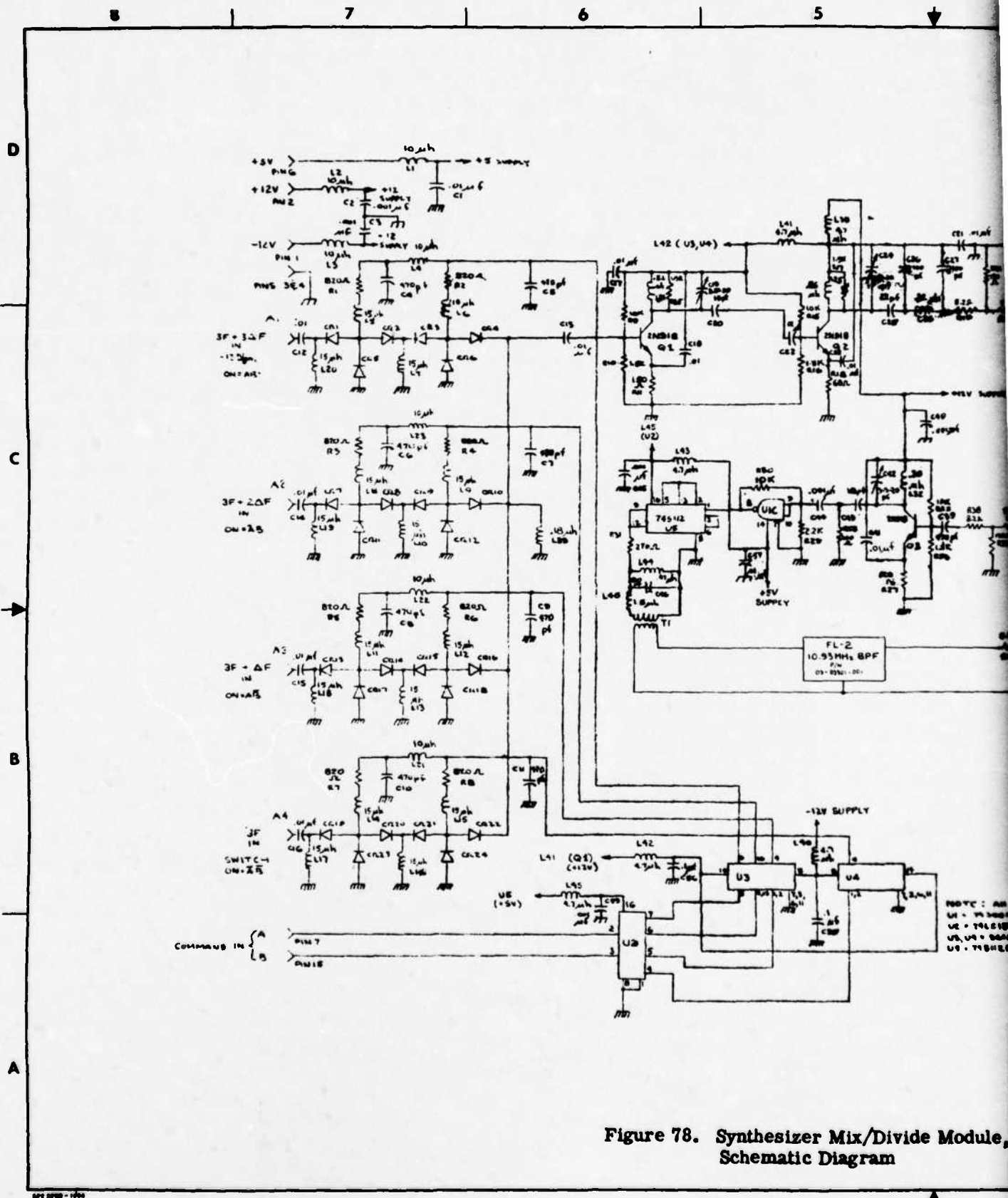
Figure 77. Synthesizer, Block Diagram

This output is padded and fed to a bandpass filter which selects the desired mixer products. The desired product is the sum frequency from the mixer. The output of the filter is again padded and applied to a buffer stage. The buffer stage output is applied directly to a logic gate. The logic gate provides limiting and squaring of the signal and in turn, drives a divide-by-four circuit composed of two JK flip-flops. The logic output is matched to 50 $\Omega$  by an LC network and the signal again is filtered by a bandpass filter. The output of the filter is again padded. The pad output then drives the next circuit board in the chain.

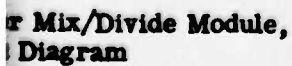
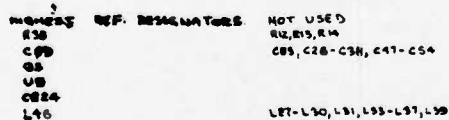
#### Schematics and Circuits

Study of the schematic shows the exact circuits used. The local oscillator drive signal is selected from one of four frequencies by diode switches composed of Diodes CR1 through CR24. Each switch provides at least 100dB of attenuation in the off-state and around 4 - 6dB of loss when on. Losses are a function of drive power and represent a compromise between the amount of loss and the drive current available. Under the conditions chosen driver current is approximately 3 milliamperes per diode with the losses based on an input level of -10dBm. The common point of the switch is at L39 and C13 with L39 actually being part of the input circuit for Q1.

Stages Q1 and Q2 provide about 40dB of gain. The output of Q2 is filtered and padded to provide a pure 50 $\Omega$  signal source.



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REVISIONS									
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			APPROVED					
APPLICATION		SCALE 4/1		SHEET				

A 3dB pad is used which makes the local oscillator drive level +16 to +17dBm at midband. At band edges drive level will drop off to +12 or +13dBm. The gain budget calls for a 0dBm signal into the synthesizer. The power splitter board provides a maximum loss of -13.6dBm. The switches add another 6dB which makes the level into Q1 around -20dBm. With at least 40dB of gain provided by Q1 and Q2 the level at the input of the bandpass filter is a nominal +20dBm. Filter loss is negligible and the pad reduces the level to +17dBm. The mixer requires +13dBm and the higher order intermodulation products are reduced somewhat with higher drive levels.

The other mixer input is from the preceding card or from the reference generator for the circuit board in synthesizer slot A1. The output of the mixer is padded with a 3dB pad which in turn, drives a bandpass filter tuned to the mixer sum frequency. The bandpass filter is a 7MHz wide filter tuned to a center frequency of 43.5MHz. The output of this filter is matched with a 3dB pad to a buffer amplifier Q3. The desired signal level from the mixer is -16dBm. The pads drop this level to -22dBm and the filter adds another 1 - 2dB of loss. The buffer provides a little over 20dB of gain which makes the input level to U1 around -3 to -4dBm. U1 provides two functions. It acts as a limiter to the signal and it also provides the correct driving waveform to the divide-by-four circuit. The divide-by-four function is provided by U5. Both U1 and U5 are Schottky-clamped TTL logic.

These devices have an operating speed up to 80MHz. The output of U5 is matched down to  $50\Omega$  by means of network L44, C46 and L46. Resistor R31 is used to stabilize the dynamic impedance of U5 to make it look like approximately  $400\Omega$ . The network then matches  $50\Omega$  to  $40\Omega$  with the loaded or operating Q of 6. Transformer T1 is a 1:1 matching transformer which is used to control ground loops on the circuit board. This transformer drives a bandpass filter 1.6MHz wide centered around 10.93MHz. The filter output leaves the card via a 3dB pad. This pad is again for mixer matching purpose as this output drives the next succeeding circuit board mixer.

The twelfth circuit board is very similar with a few minor changes. The output matching network is tuned to a center frequency of 43.5MHz. The output filter FL-2 has been changed in frequency. This circuit board output is used to drive a buffer amplifier modified for operation at 43.5MHz rather than 70MHz. The buffer amplifier except for required tuning and bandwidth changes, is identical to the 73.8MHz building block module. This module provides the required output of +12dBm as well as additional filtering of the output signal. The signal appears at J6 on the synthesizer chassis.



#### 4.2.4 Results

This section shows the final results obtained with the synthesizer. Section 4.2.4.1 shows the test procedure used to demonstrate performance and Section 4.2.4.2 shows actual photographs of the synthesizer in action.

##### 4.2.4.1 Synthesizer Test Procedure

It shall be the purpose of this procedure to provide a method for the testing of the modem building block synthesizer. The following tests will be run: Frequency, Settling Time, Switching Capability, Spurious Responses, and Spectral Purity. The following test equipment will be required:

- (1) Null Network
- (2) Frequency Counter
- (3) Discriminator
- (4) Spectrum Analyzer
- (5) Reference Generator or a substitute to consist of  
four crystal oscillators and a divide-by-three circuit
- (6) Test Chassis
- (7) Double Balance Mixer (two each)
- (8) Oscilloscope
- (9) Function Generator
- (10) Wide Band Amplifier
- (11) Step Attenuator
- (12) Noise and Field Intensity Meter
- (13) Assorted Filters, 50 $\Omega$  5MHz Low Pass, 21.4MHz 1MHz  
Bandpass, 43.5MHz 7MHz Bandpass

#### 4.2.4.1.1 Frequency Test

Connect the synthesizer to the test box and apply power. Drive the inputs with a signal of 0dBm at J1-J4 and -10dBm at the input to J5.

Connect the frequency counter to J6. A measurement of twenty-four frequencies will be made. Change the MSB switch and note the frequency change. Place the switch back to the "0" state and change the second switch to a "1" state. The frequency change should be one-half the previous change. Repeat for all switches noting that each change is exactly one-half the previous change.

#### 4.2.4.1.2 Settling Time

Disconnect the drive to J4 and J5. Use power splitters and an attenuator and reconnect to J4 and J5. The attenuator is in the line to J5. Increase the generator output driving J5 to +10dBm. Set the attenuator for 17dB attenuation. The other splitter output drives a double-balanced mixer. Connect the extra signal from the J1 drive to the other mixer port. The IF output of the mixer needs to be bandpass filtered. It is then applied to the second mixer. The other input to the mixer is from J6. The output of this mixer is lowpass filtered and applied to the vertical input of an oscilloscope. A function generator is used to switch-bit 12. The function generator is used to trigger the oscilloscope. The display on the scope will show settling time as it will either be a beat note or a DC level when the synthesizer switches

frequencies. The time required from the start of the sweep to stabilization of the DC level will be the settling time.

#### 4.2.4.1.3 Switching Capability

The test is to demonstrate the frequency agility of the synthesizer. The test is run by logic in the control box. A function generator supplies the required clock. The signal source and control box are connected as before except the switches for Bits 13-20 are set to a "1" level. The logic is then connected which throws the switches electrically in a binary sequence. The results will be a ramp which increases in frequency in 256 steps. Total amplitude will be 400KHz peak-to-peak. The output of the synthesizer will drive a wideband discriminator. The output of the discriminator will drive an oscilloscope which can be used to evaluate performance. The oscilloscope should be triggered on the divided signal in the control box.

#### 4.2.4.1.4 Spurious Responses

The synthesizer is connected to a signal source and the control box. The output from J6 is connected to a spectrum analyzer through a null network. The null network provides a sharp notch in the response. The network is necessary since the analyzer's dynamic range is less than the required 100dB. The synthesizer output is set to the notch frequency and the network is adjusted for maximum null of the signal. The analyzer is then tuned over the spectrum to look for spurious signals. The analyzer is calibrated by disabling the network, attenuating the signal 100dB, and noting the signal level.

The network is reconnected and the attenuation is removed, and the analyzer set for maximum sensitivity. The unnull level is the -100dB reference point. With the null network restored, the analyzer is then used to search for spurious responses. Any level above the -100dB reference is exceeding the design goal level of -100dB below the output frequency.

#### 4.2.4.1.5 Spectral Purity

This test will require the use of a spectrum analyzer with a VHF-RF head. The synthesizer will need a signal source composed of either a reference generator or signal generators that provide the necessary signals. The output (J5) of the synthesizer feeds the spectrum analyzer. The analyzer is set with the main signal of the synthesizer in the center of the display. The analyzer is set to the narrowest bandwidth position with a 10Hz video filter. The display is set for full scale at the top of the screen. The dispersion control is set at its narrowest dispersion initially. The display is then examined to determine the sideband content of the carrier. Since the specification is for a 1Hz bandwidth, 10dB will be subtracted from the display. The level of spurious can then be measured to the full carrier amplitude and compared with specification requirements.

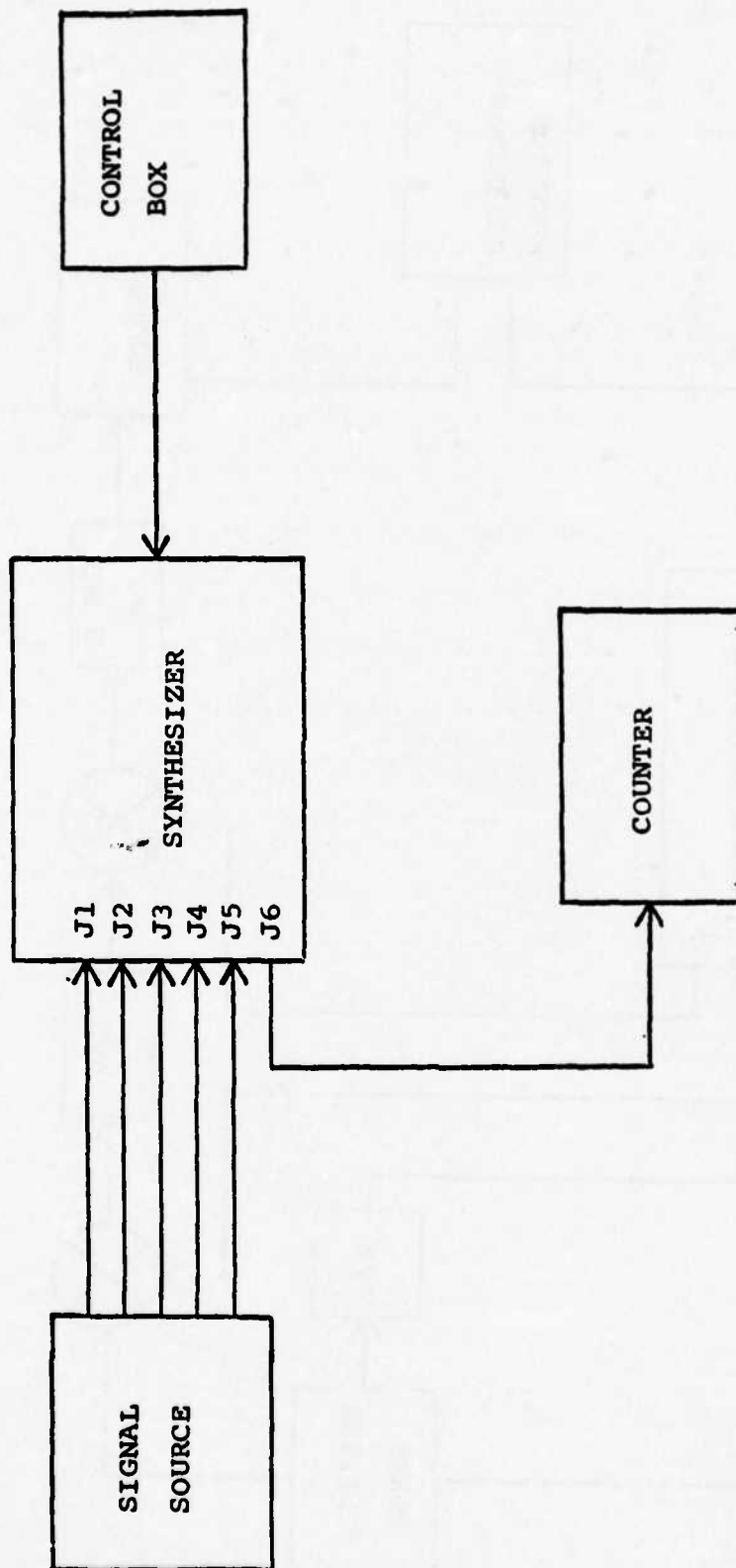


Figure 80. Synthesizer Frequency Test, Bench Test Setup

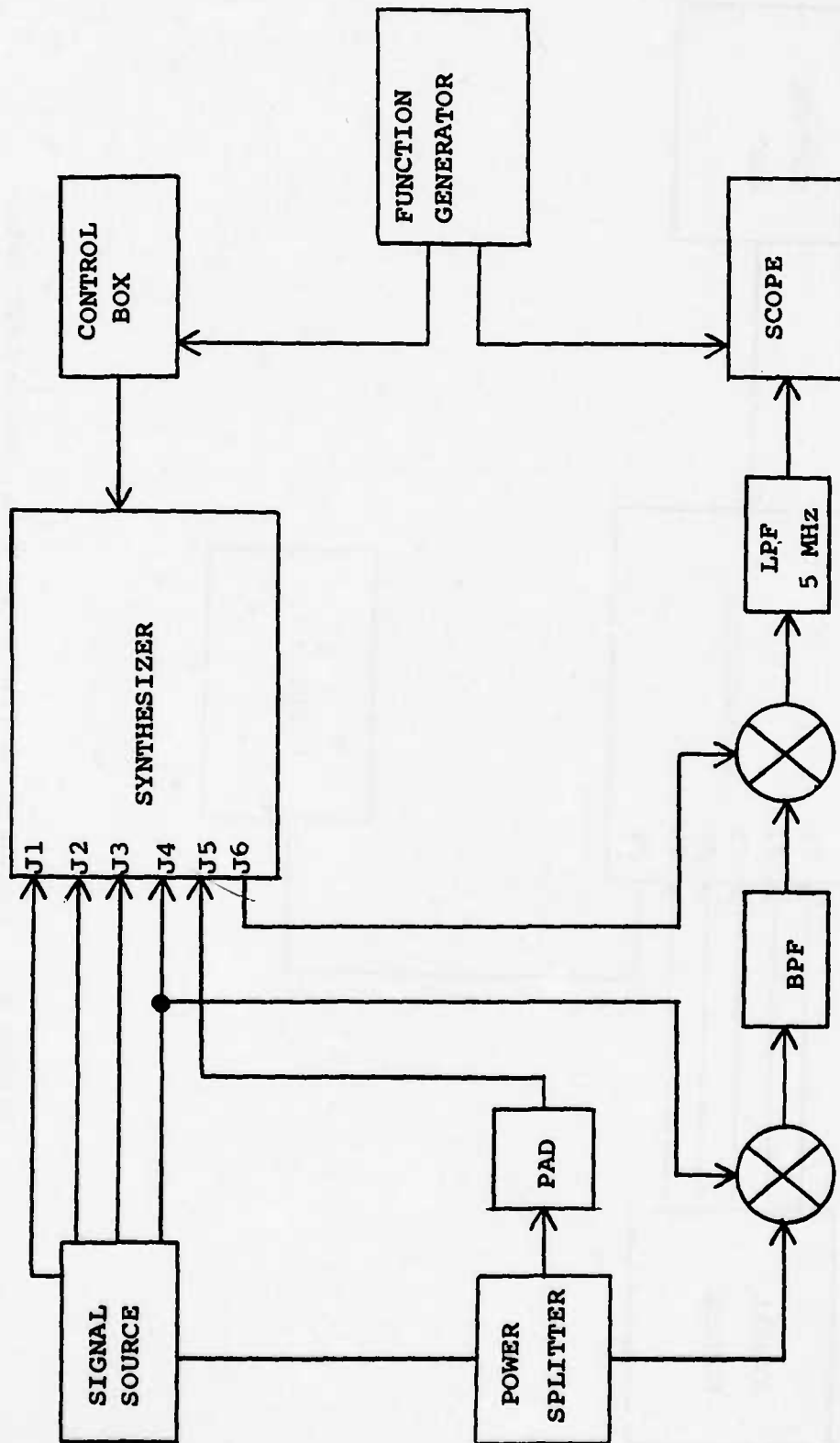


Figure 81. Synthesizer Settling Time Test, Bench Test Setup

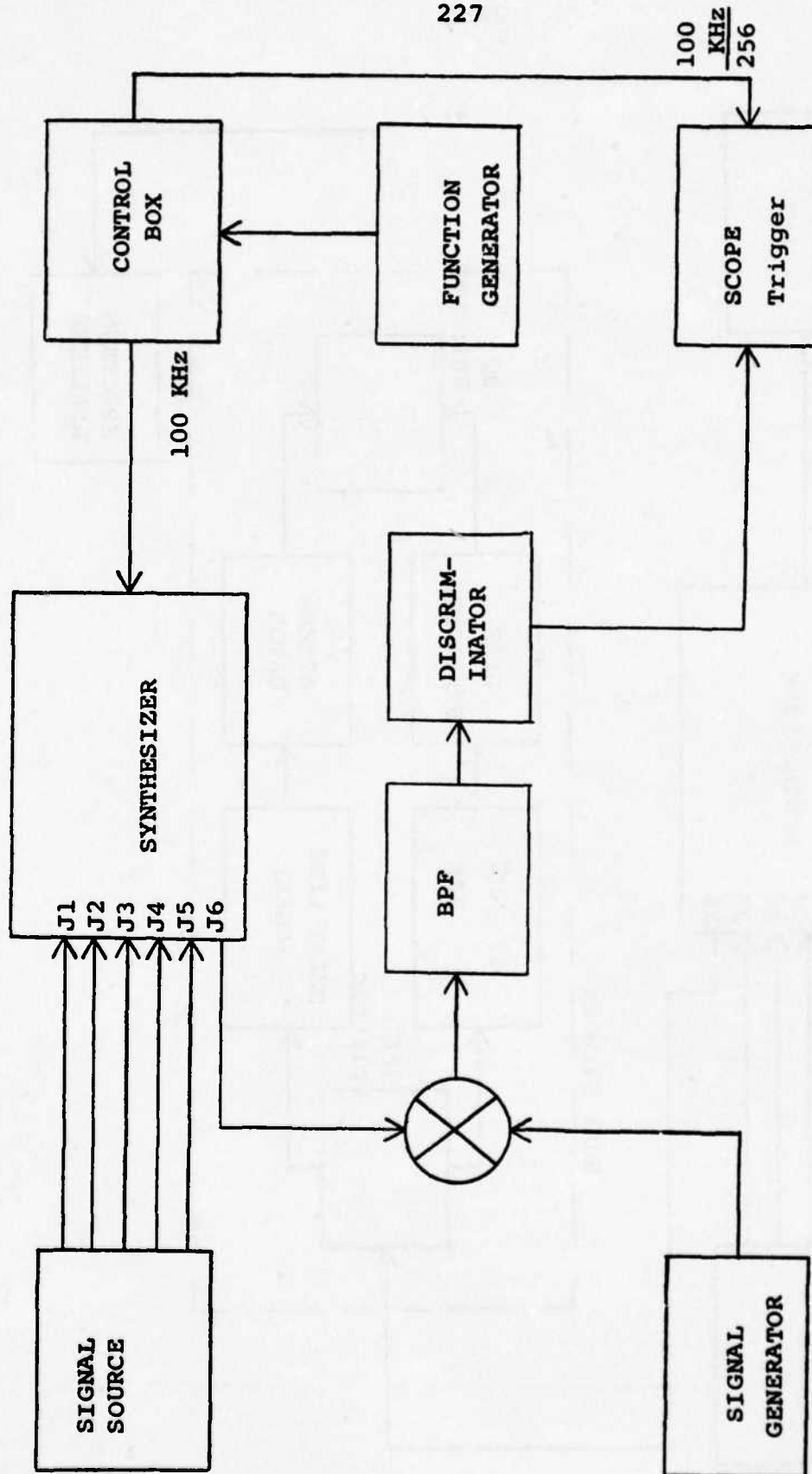


Figure 82. Synthesizer Frequency Agility Test, Bench Test Setup

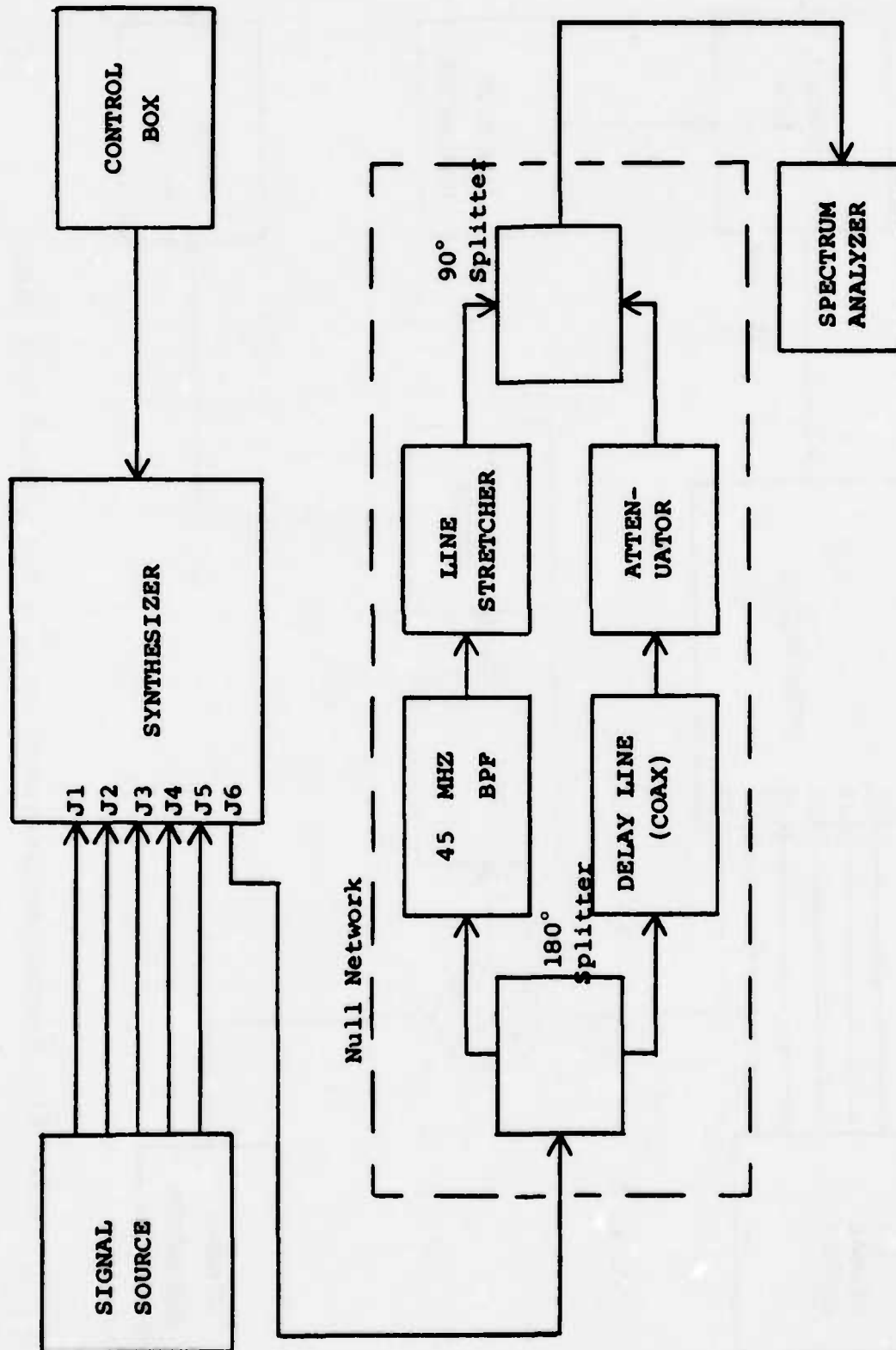


Figure 83. Synthesizer Spurious Response Test, Bench Test Setup

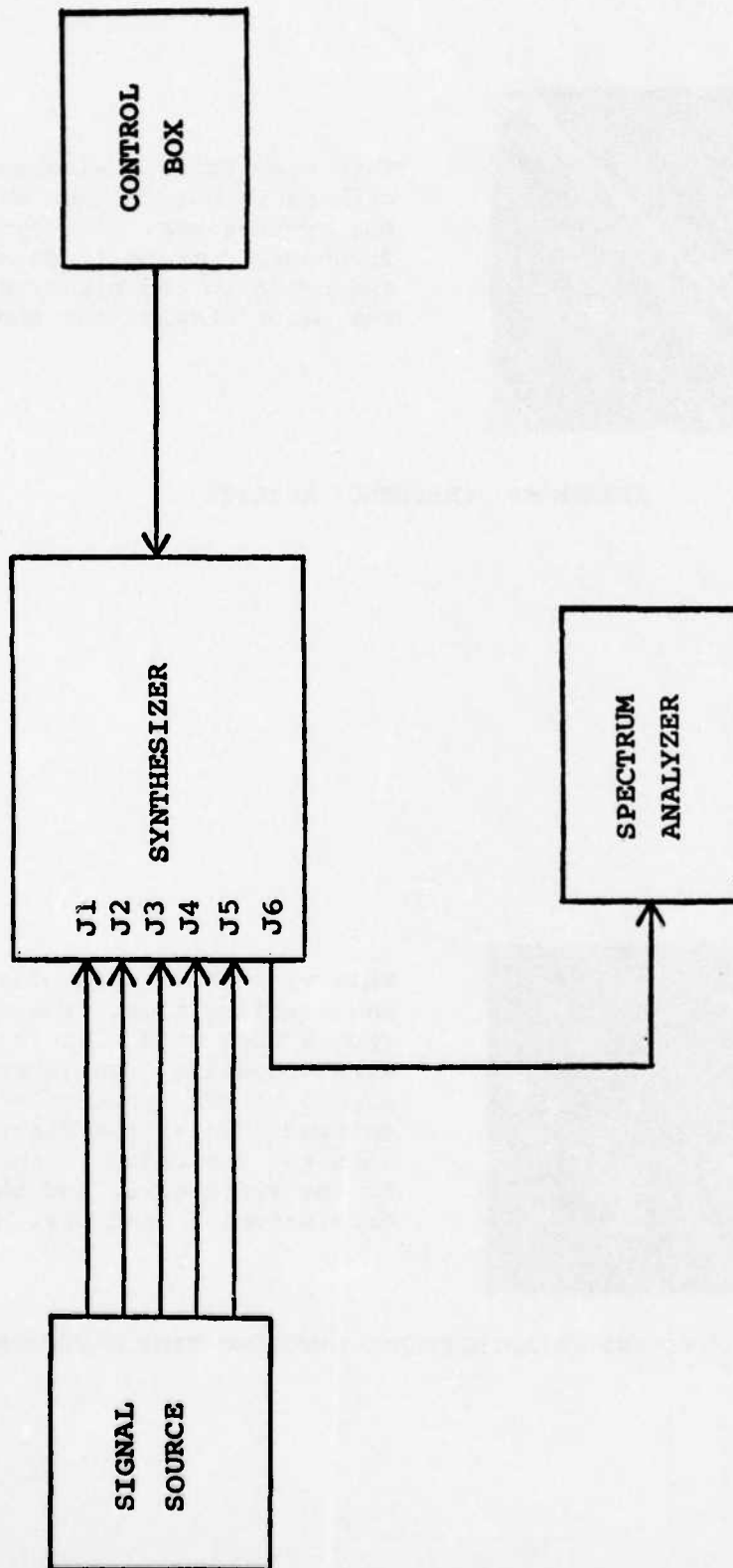
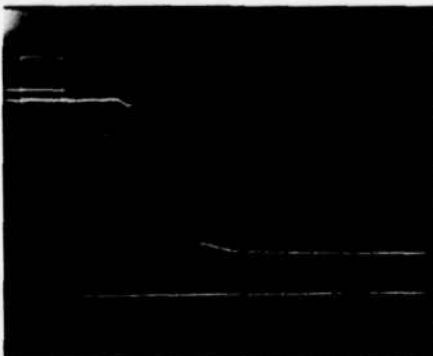


Figure 84. Synthesizer Spectral Purity Test, Bench Test Setup



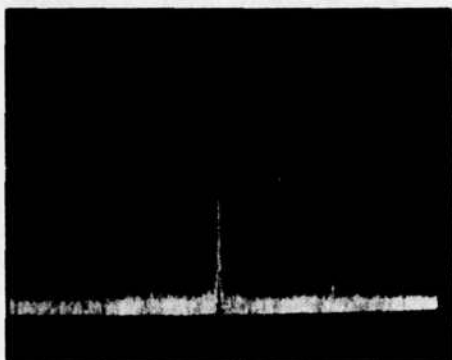
This view shows a wideband discriminator output when driven by the synthesizer. The synthesizer frequency command lines are being exercised in 256 binary steps. The major step at the end is 400KHz.

FIGURE 85 FREQUENCY AGILITY



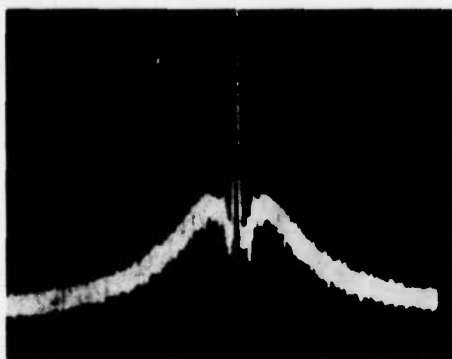
This view shows switching capability and settling time. The signal is from a wide band discriminator. The first negative edge is the command signal to the synthesizer and the delayed edge is the discriminator output. The delay is the total due to the synthesizer and the discriminator. 2  $\mu$ sec/div. horizontal.

FIGURE 86 SWITCHING CAPABILITY AND SETTTLING TIME WAVEFORM



This is the output spectrum of the synthesizer at center frequency. Top scale (oDb log) is at -30Dbc. 1MHz/div. horizontal and 1KHz IF bandwidth.

FIGURE 87 SYNTHESIZER OUTPUT SPECTRUM



This is a view of the spectral purity. Top scale (oDb log) is at -30Dbc. 20KHz/div. horizontal, 300Hz IF bandwidth, 10Hz video filter.

FIGURE 88 SPECTRAL PURITY

#### 4.2.5 Operating Instructions

Operation of the synthesizer is relatively simple. Power required is  $\pm 12\text{V}$  at 1 amp for each voltage and +5 volts at 1 ampere. The following table shows required inputs and associated levels.

Table 13. SYNTHESIZER INPUTS AND LEVELS

<u>INPUT</u>	<u>SIGNAL</u>	<u>LEVEL</u>
J1	$F+3\Delta f$	0dBm
J2	$F+2\Delta f$	0dBm
J3	$F+\Delta f$	0dBm
J4	F	0dBm
J5	$\frac{F}{J}$	-10dBm
J6	Output	+12dBm
P1-1 thru P1-24	LSB MSB	$T^2L$ $T^2L$
P1-25	-V	-12VDC
P1-26	GND	--
P1-27	+V	+12VDC
P1-28	+V	+5VDC
P1-29	GND	--
P1-30	GND	--

With proper power and signals applied, inputs on Pins 1-24 of P1 can be used to command any frequency desired. These commands are standard levels. The frequency will be

$$f_o = 4f + \sum_{i=1}^{12} \frac{n\Delta f}{4(i-1)} \quad n = 0,1,2,3$$

The versatility of the synthesizer can be shown by operating 8 of the bits in a binary sequence. This will produce a ramp which can be seen in a discriminator.

#### 4.2.6 Modification Instructions

Other frequencies and bandwidths should be easily obtainable. The input switches are not frequency sensitive and have been tried at frequencies extending on up to 250MHz. To change the synthesizer frequency new tuning networks need to be incorporated in the filters and buffer stages. Required changes consist of L24, C18, C19 and C20 in the Q1 stage; L38 C24, C25 and C26 in the Q2 stage; L32, C42 and C43 in the Q3 stage; Network L44, L46 and C46 at the output of U5, FL-1 and FL-2. Also, the LPF at the output of Q2 may need changing. It consists of C26, C27 and L26.

A procedure to change Q1's tuning will also work with the other stages on the circuit board. To change frequency, the devices new Y parameters are picked up from a data sheet or measurements. Next the stability is checked. The following formula is used.

$$C = \frac{Y_{12} Y_{21}}{2g_{11}g_{22} - R_e(Y_{12} Y_{21})}$$

if  $C \leq 1$  the device is unconditionally stable. If this is not the case, certain precautions must be observed during the design process. Next, a  $R_L$  is assumed around  $800\Omega$  to  $1K\Omega$ . Experience has shown this to be a reasonable loading value on a 2N918 stage at these frequencies. For the matching circuit used there is an equivalent parallel circuit. This equivalent circuit must load the stage with the selected collector resistance. The required series  $C$  to match  $50\Omega$  to the collector may be found from the following:

$$X_s = R_s \sqrt{\frac{R_p}{R_s} - 1}$$

This will then transform the  $50\Omega$  load to the desired collector load. The equivalent circuit then appears like the following:

$$R_p = R_s + (1 + Q^2), \quad Q = \frac{X_s}{R_s} \quad X_{cp} = \frac{R_s R_p}{X_s}$$

The operating  $Q$  is determined by  $\frac{R_p}{X_L}$  and is set for the desired bandwidth by choosing  $X_L$ . Sufficient capacitance is then added so that the circuit resonates to the desired frequency.

This should complete tank circuit modifications. When this is done, a new stability check should be made on the device.

For this check both load and source impedances are included in the formula.

$$K = \frac{2 (q_{11} - G_s) (q_{22} + G)}{Y_{12} Y_{22}}$$

The value of  $G_s$  chosen can be 50  $\Omega$ . (.02 milliohms). If the value of  $K > 1$  results, then the circuit will be unstable. An adjustment to the circuit will be needed. Usually for an unstable operating condition all that will need to be done is to change the collector load to a smaller value. Matching can be done to the input of the device but it was felt not to be necessary for this application. The input impedance can be calculated using the following formula:

$$Y_{in} = Y_{11} - \frac{Y_{12} Y_{21}}{Y_{22} + Y_L}$$

This procedure should work with any of the stages on the circuit board. Other changes to the board for other frequencies involve changing the filters FL-1 and FL-2. The new filters will require tuning to the new frequency and setup for the new bandwidth. The only other circuit that requires modification is the logic output network L44, L46 and C46.

This network matches and tunes at the board output frequency. The match is from a  $50\Omega$  line to  $400\Omega$ . The Q is based on the required bandwidth. Matching and tuning is done by the same method as was used for the transistor collectors at Q1, Q2 and Q3. The only difference between the transistor stages and this network is that an inductor is used for the matching element rather than a capacitor.

#### 4.3 CONCLUSIONS

The goals of channel quantity, channel spacing, settling time and spectral purity were met or exceeded. Spurious response goals were more difficult to meet and a relaxation was necessary. Spurious response goals need analysis to determine if the goal is realistic and if realistic then what changes are necessary in order to meet the requirement. Existing performance meets the -80dbc goal. To achieve this, many layout modifications were made to the mix/divide boards to improve performance. This entailed careful study of ground loop paths and their effects on adjacent circuitry. Once the boards were performing satisfactorily, chassis design considerations were made as to shielding requirements and shielding techniques, and a chassis was constructed. Some additional work was required on the finished chassis to eliminate ground loops which caused poor spurious performance. At this point the -80dbc specification was achieved.

Shielding requirements and circuit needs were allowed to dictate physical size. Some size changes could be made with additional module changes and greater study of ground loop techniques. Chassis changes to produce 140 to 150dB of isolation are required in order to meet the original design goal of -100dBc. Chassis ground loops were responsible for some of the spurious responses in the region of -90dBc. One or two other spurs are due to mixer characteristics and these need re-evaluation to obtain better mixers for better performance. Another approach to mixer products is to choose alternate mixer frequencies so that the only mixer products in the passband are the desired ones along with high order products only. High order products are usually fairly low in level and limiting techniques will lower them even further.

## SECTION V

## REFERENCE GENERATOR

5.1 INTRODUCTION

The reference generator is needed to provide the reference frequencies for the AFAL mix-divide synthesizer. The five references required must be precise in frequency, coherent with each other and with an external 1MHz frequency input. The importance of absolute zero frequency error, relative to the 1MHz input, can be appreciated by considering the extremely small output frequency increments that the synthesizer develops.

Very small average frequency errors in the reference frequencies would not only be translated into synthesizer output frequency errors, but could easily destroy output frequency monotonicity.

Phase noise and spurious frequency requirements of the synthesizer are very stringent. This, coupled with the coherence requirement, led to the decision to use voltage-controlled crystal oscillators within phase-locked loops as the frequency determining circuits.

## 5.2 BASIC BLOCK DIAGRAM OF REFERENCE GENERATOR

Figure 89 indicates the basic scheme used. Each frequency,  $3F$  to  $3F+3\Delta F$  is developed independently of the others. The 1MHz source is a common input to each phase-locked loop. This source must have excellent frequency stability and accuracy in order to guarantee the same of the frequency synthesizer. The 1MHz reference is not included in the reference generator, but is expected to be the external oscillator used as the reference in the system in which the synthesizer is to be used.

Figure 89 also indicates that there are five output frequencies;  $F$ ,  $3F$ ,  $3F+\Delta F$ ,  $3F+2\Delta F$  and  $3F+3\Delta F$ . The synthesizer uses these frequencies to produce an output range from  $4F$  to  $4F+4\Delta F$ .

Figure 90 is a block diagram of the individual phase-locked loop. Each of the output frequencies is related to the 1MHz source by a common 12.5 KHz division. Thus, the phase detector frequency was selected to be 12.5 KHz. The reference input to the phase detector is developed by dividing the 1MHz source through the use of a "divide-by-80" digital divider.

The VCXO output at  $3F$  is applied to a digital mixer that translates the signal down to the difference between  $3F$  and the closest 1MHz multiple.

The mixer output frequency is digitally divided to 12.5KHz by a variable modulus divider, whose modulus depends on the particular output frequency. A loop filter is included to set the loop's bandwidth to a value, compatible with acquisition and noise requirements.

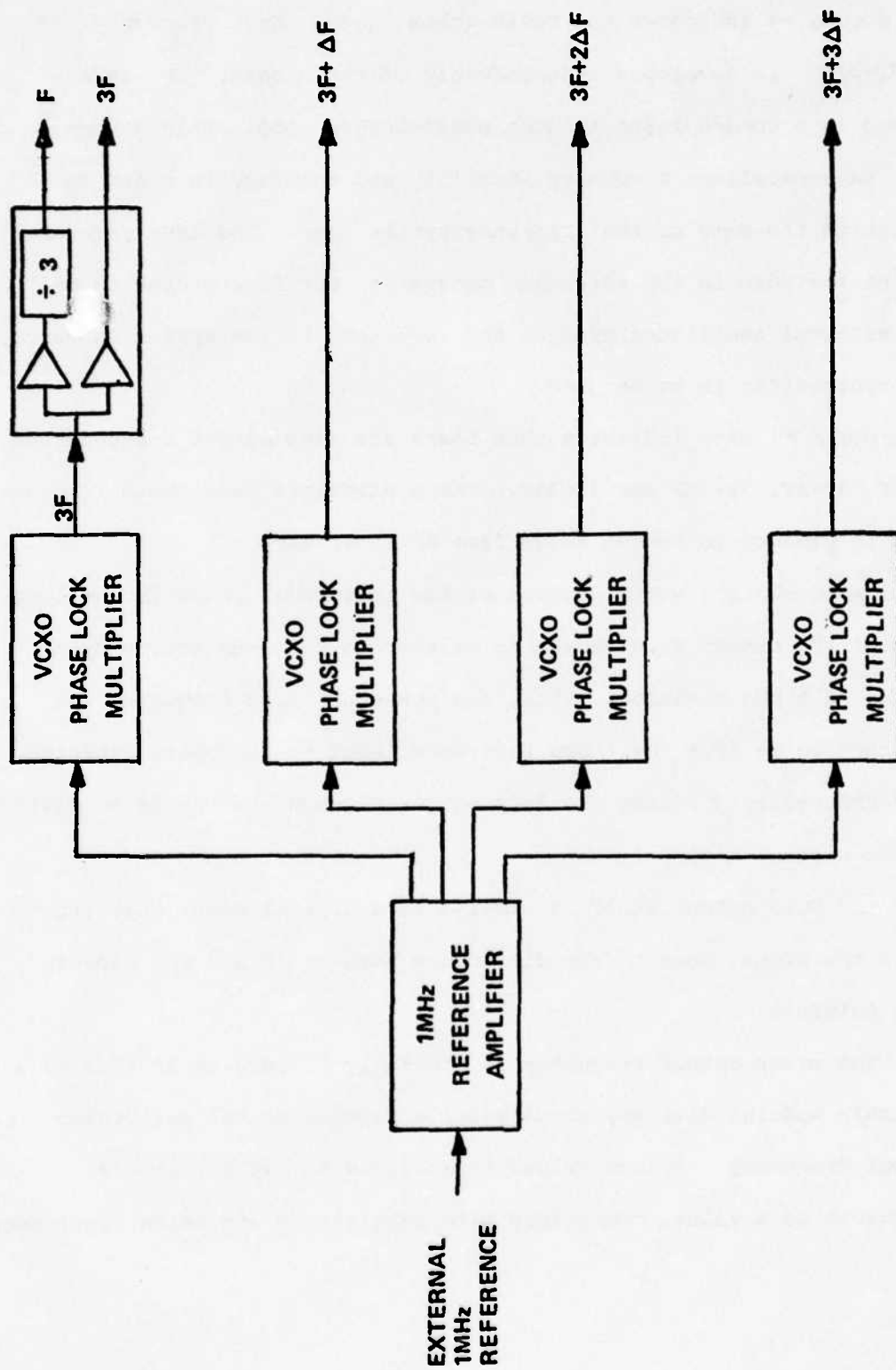


Figure 89. Reference Generator, Block Diagram

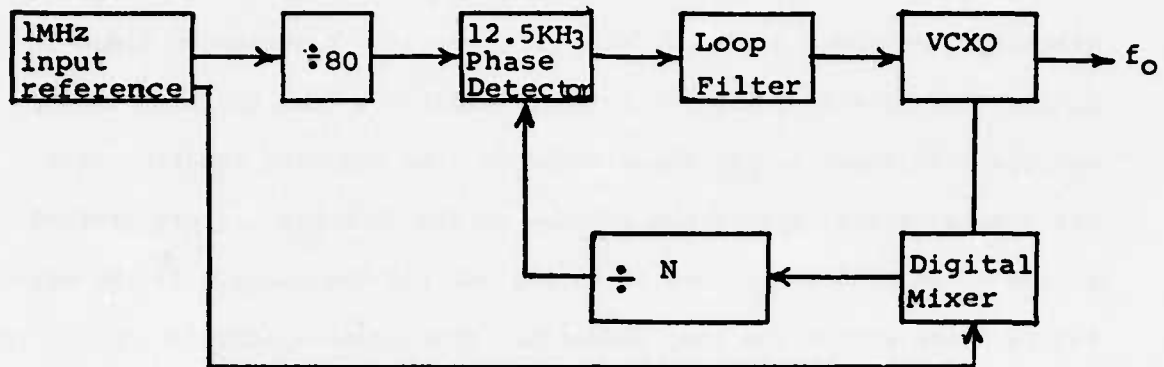


Figure 90. Single Output Frequency PLL, Block Diagram

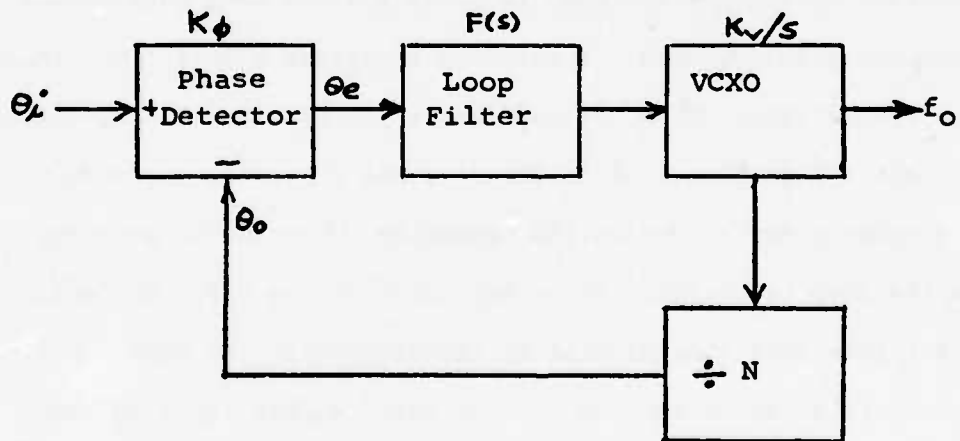


Figure 91. Mathematical Model of a phase lock loop

### 5.3 DISCUSSION OF SYSTEM OPERATION

The basic tasks of a phase-locked loop are acquisition and tracking. At the instant of "turn on", the loop experiences a mis-tuning ( $\Delta\omega$ ) between the phase detector reference (the positive input) and the VCXO input to the phase detector (the negative input). This mis-tuning exists because the voltage on the VCXO has not yet arrived at the value needed, to tune it to the desired frequency. If the mis-tuning falls within the loop bandwidth, then instant acquisition occurs, followed by a settling transient. If the mis-tuning is outside the loop bandwidth then, instead of instant acquisition, a beat note exists whose frequency equals the mis-tuning ( $\Delta\omega$ ). Because of the negative feedback present, the beat note becomes distorted developing a broad positive portion and a narrow negative portion (for a negatively mis-tuned VCXO). The integrating effect of the loop's filter accumulates the DC voltage needed to tune the VCXO. When this voltage is reached the VCXO is tuned and the beat note ceases. The loop has thus acquired. A settling transient also follows this form of acquisition. Thus, to facilitate acquisition, a large bandwidth loop is desirable. After the loop has acquired, the VCXO will track frequency deviations of the reference, which occur at rates within the loop bandwidth. Thus, any noise in the reference source or in the reference channel will be transferred to the VCXO. Similarly, any FM noise in the VCXO, which falls within the loop bandwidth, will be tracked out by the loop. Thus, the loop has a low pass reference transmission characteristic, i.e. from source to loop output; a high pass VCXO transmission characteristic, i.e. from VCXO to loop output.

In developing a reference channel, it is inevitable that a certain amount of noise is built into it. Thus, the reference that exists within the phase detector is not as quiet as the frequency source. When a voltage-controlled oscillator is noisier than the reference channel, then the loop bandwidth should be expanded to track out the VCO noise. If the VCO is quieter than the reference channel, then the loop should be made narrow to impart only the average frequency information to the VCO and not contaminate the already quiet VCO by forcing it to track the noisier reference channel.

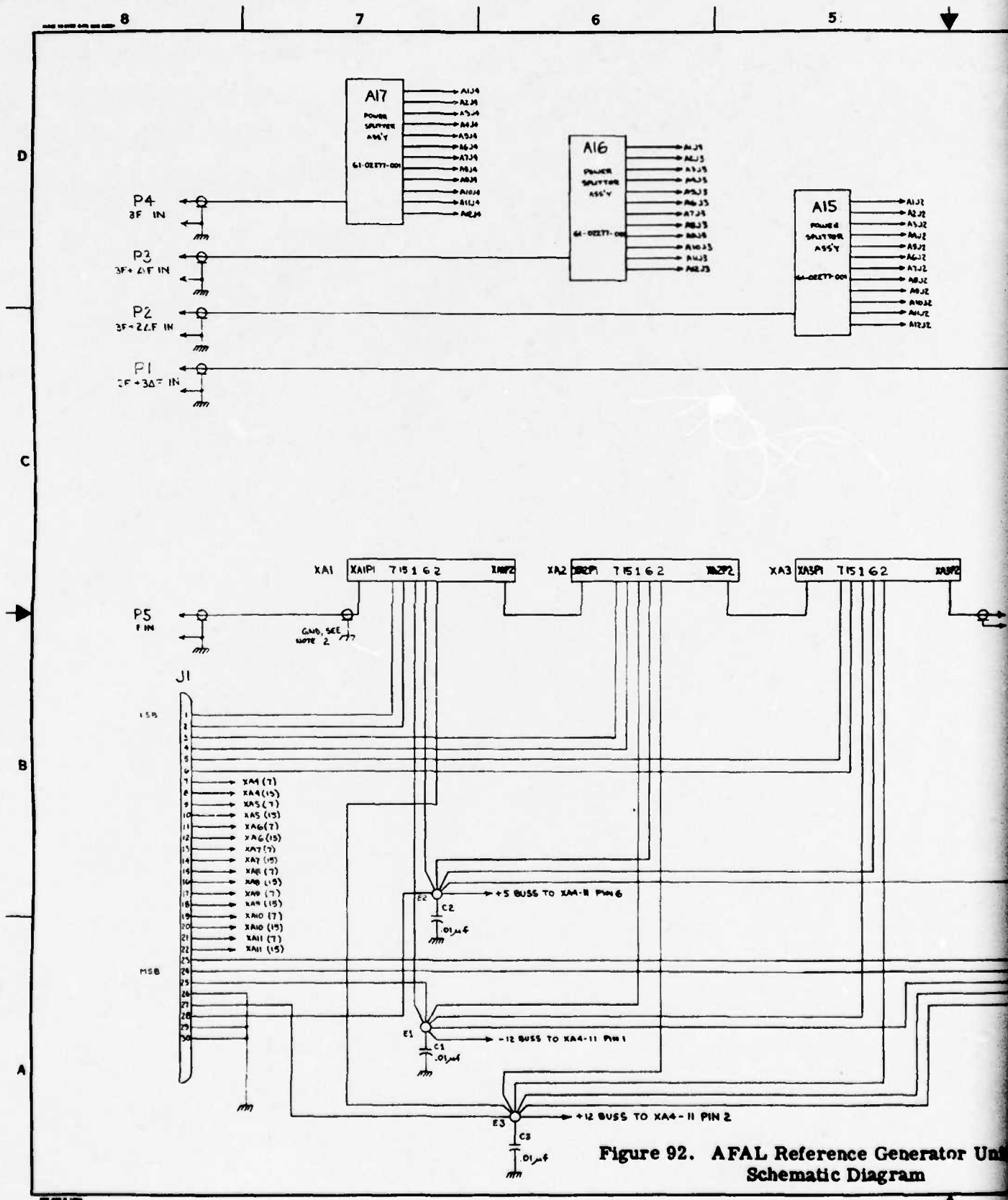
The latter is the case with the reference generator. The output oscillators are themselves crystal oscillators and are included into a phase-locked loop not to impart low noise characteristics, which they already have, but for synchronization. Thus, the reference generator loops have bandwidths of about 12Hz so that beyond that frequency the output noise characteristics will be largely that of the output crystal oscillators. Below 12Hz the oscillators will follow the source frequency in phase coherence.

#### 5.4 DISCUSSION OF SCHEMATICS

The following is a description of the schematic as it applies to the block diagram, shown in Figure 90.

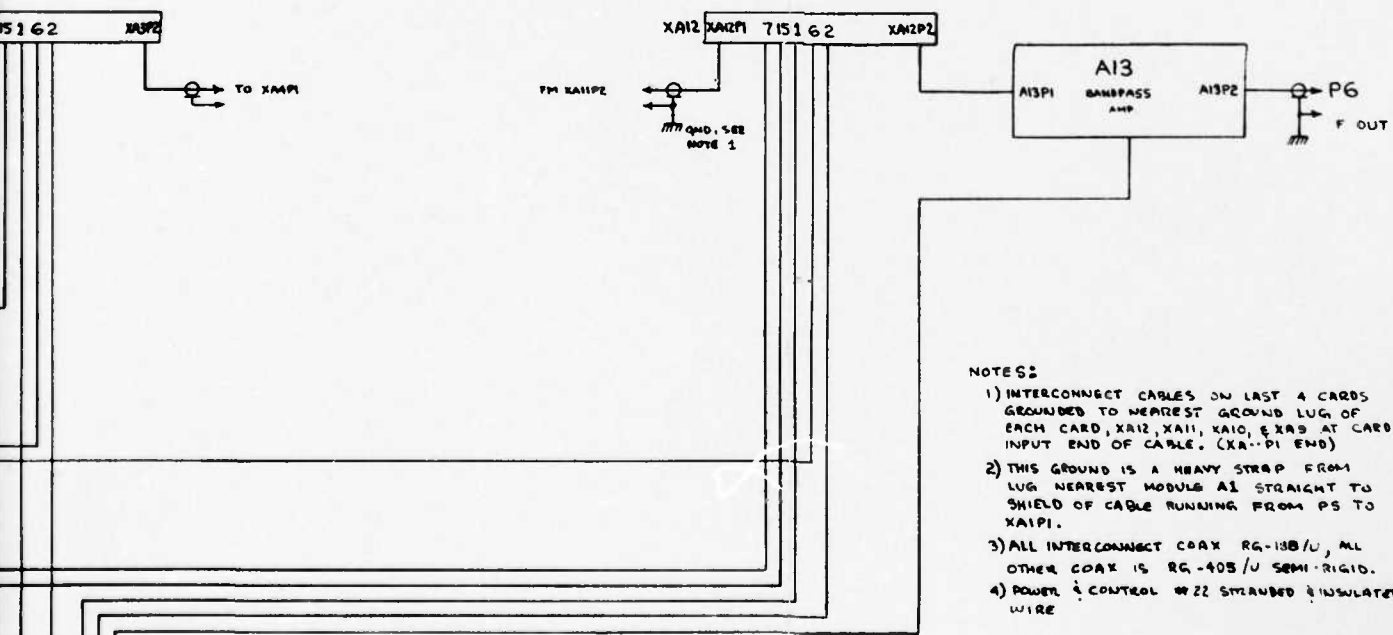
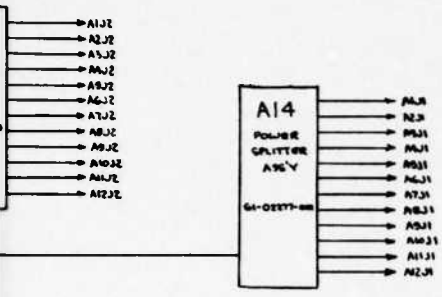
The basic crystal oscillator is the circuit of Q1. The crystal, XL1, operates on the third overtone at  $3F$ . To suppress oscillation at the fundamental frequency of  $F$ , L1 and C4 parallel resonate at  $3F$ . Amplifiers Q2 and Q3 provide power amplification and reverse isolation from other signals existing in the oscillator's load. These signals originate in the counters and the external synthesizer which are ultimately driven by the oscillator board. To prevent the synthesizer and internal counter signals from contaminating each other, separate drive stages (Q4 and Q5) are used.

The  $3F$  frequency enters the digital mixer (U2) where it is clocked in by a 1MHz clock applied to Pin 3. This mixer, which is a high-speed "D" flip-flop, has an output frequency equal to the difference between  $3F$  and the closest 1MHz multiple. In this case it is  $(3F - Q\text{MHz})$ . (Note that for a frequency of  $3F + 2\Delta F$  MHz the closest 1MHz multiple is above  $3F + 2\Delta F$ , so the mixer's output is  $(P+1)\text{MHz} - (3F + 2\Delta F)$ , not  $3F + 2\Delta F - P$  MHz.) The  $3F - Q$  MHz signal proceeds to Counters U9 and U10, which together provide division by "N". The counter's output is applied to R44 of the phase detector and thus Q8 is switched at a 12.5KHz rate to which L6 and C29 are tuned. As a consequence, a 5V peak sinewave is developed at the base of Q9. Note that R47 and R46 cause this signal to have a small positive DC offset which is, subsequently, amplified (U8) to 4VDC, the nominal VCXO tuning voltage.



2

4	3	2	1
245 (246 blank)		REVISIONS	
ZONE LTD	DESCRIPTION	DATE	APPROVED



- NOTES:
- 1) INTERCONNECT CABLES ON LAST 4 CARDS GROUNDED TO NEAREST GROUND LUG OF EACH CARD, XA12, XA11, XA10, & XA9 AT CARD INPUT END OF CABLE. (XA--PI END)
  - 2) THIS GROUND IS A HEAVY STRAP FROM LUG NEAREST MODULE A1 STRAIGHT TO SHIELD OF CABLE RUNNING FROM P5 TO XA1P1.
  - 3) ALL INTERCONNECT COAX RG-138/U, ALL OTHER COAX IS RG-405/U SEMI-RIGID.
  - 4) POWER & CONTROL WIRE STRANDED & INSULATED WIRE

Generator Unit No.2,  
Diagram

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES 2 HOLE DIA TOLERANCES UP +.000   .001 DIA DOWN -.000   .000 DIA .000 DIA - .000   .000 DIA - .000 REMOVE BURRS BREAK SHARP EDGES .010 ± .010 MATERIAL		CONTR 1000000005 NO 10000000	<b>ELECTRONIC COMMUNICATIONS, INC</b> ST PETERSBURG, FLORIDA - A SUBSIDIARY OF NCR	
		DWS B.J. BLACK CWD CWD CWD B.J. BLACK RT/BLACK APPROVED MAINT ENDOR APPROVED	<b>SYNTHESIZER WIRING DIAGRAM</b>	
HEAT ADDY APPLICATION	PMS SYNTHESIZER USED ON FINISH	SIZE CODE BENT NO <b>D 00724</b>	05-08211-000 SCALE SHEET	

105-08211

A

Transistors Q9 through Q12 form a low output impedance current driver which isolate the sinewave from the following sampling process. Analog switch U7 receives a 12.5 KHz sample pulse from the "divide-by-80" counter (U4, U5, U6) which divides down the 1MHz system reference frequency. A 12.5 KHz sinewave is normally impressed on C34, except for the 4 $\mu$ second sample period during which Pin 2 of U7 falls low. At the time C34 is disconnected from the current driver and internally connected to C35, it re-adjusts its voltage to agree with the most recent sampling of the sinewave. In this way the voltage on C35 is correlated to the phase relationship between the 12.5 KHz sinewave and the 12.5 KHz sample pulse (U7, pin 2). This voltage is amplified by U8 to a 4-volt tuning voltage which drives the VCXO.

The loop dynamics, natural frequency and damping factor, are set by the lag-lead filter, R1, R2 and C1. The VCXO is controlled by the voltage at the junction of R1 and R2.

## 5.5 TEST PROCEDURE, DATA AND TEST METHODS

### 5.5.1 Output Frequency

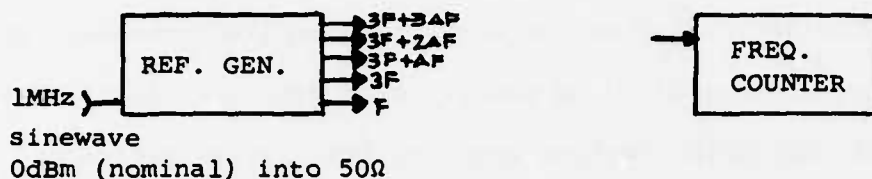


Figure 93. Reference Generator Output Frequency Test,  
Bench Test Setup

- A. Connect the 1MHz input reference to a frequency counter and adjust it to 1000001Hz.  
  
Remove 1MHz from frequency counter and connect it to the reference generator, Unit 1.
- B. Turn reference generator power switch on. The frequency indicated should be about 10Hz higher than nominal, F.  
  
Connect the frequency counter to Units 2, 3, 4 and 5.  
  
The frequency indicated should be about 30 to 35Hz higher than nominal.  
  
Turn reference generator power to OFF.  
  
Record whether or not frequencies are correct.
- C. Re-adjust the 1MHz to 999999Hz. Repeat Paragraph B.  
  
The frequencies indicated should be 10Hz, and 30 to 35Hz (respectively) LOWER than nominal.  
  
Record whether or not frequencies are correct.  
  
These tests simply indicate that the reference generator can lock up to a slightly mis-tuned 1MHz source.

D) Retune the 1MHz crystal source to  $1\text{MHz} \pm 0.1\text{Hz}$ . This might more easily be done by adjusting the 1MHz source until the Unit 1 reference generator output frequency is no more than 1Hz away from nominal. Outputs F, 3F,  $3F+\Delta F$ ,  $3F+2\Delta F$ ,  $3F+3\Delta F$  should be within 3.5Hz of specification.

Record whether or not frequencies are correct.

#### 5.5.2 Power Output

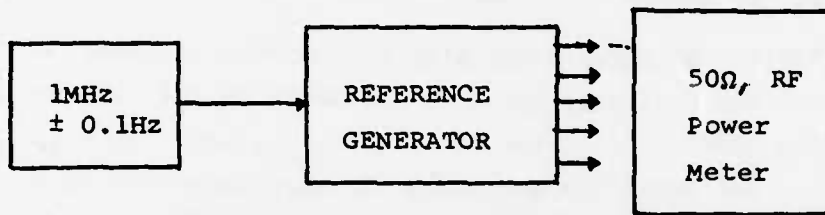


Figure 94. Reference Generator Power Output Test,  
Bench Test Setup

Measure the RF power output from Units 1, 3, 4, and 5.

(Note that Unit 1 has two output frequencies and Unit 2 does not provide power external to the reference generator)

The minimum output power should be 0dBm into 50 .

	<u>Power Output</u>
Unit 1, F output:	_____
Unit 1 3F output:	_____
Unit 3, $3F+\Delta F$ :	_____
Unit 4, $3F+2\Delta F$ :	_____
Unit 5, $3F+3\Delta F$ :	_____

## 5.5.3 Spectral Purity

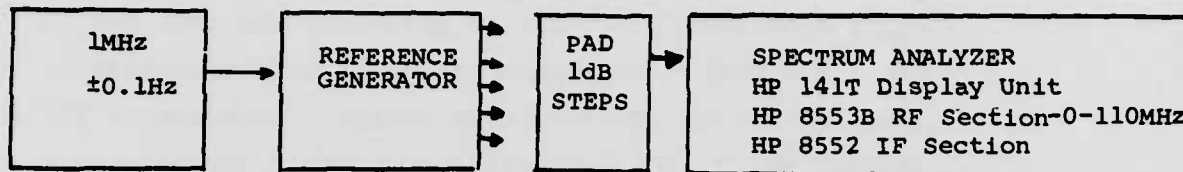


Figure 95. Reference Generator Spectral Purity Test, Bench Test Setup

## 5.5.4 Single-Sided Random Noise

This is specified in a 1Hz bandwidth. Ten Hz is the smallest bandwidth available on the spectrum analyzer. Therefore, the specification shall be translated to that measurement bandwidth as indicated below.

- . Set the RF Input Attenuator on the 8553 to 10dB.
- . Set the Log. Ref. Level on the 8552A to the -10 step and the continuous adjustment to -10.5, a total of -20.5dB log ref level (DO NOT use a -20 step with -0.5 continuous to get the same level. IF is noisier that way.) Log/Lin switch to (10dB) log.
- . Connect the reference generator output under test to the 50Ω input of the 8553. Adjust the RF Input Attenuator and the external 1dB step attenuator so that the indicated peak coincides with the 0dB display reference.
- . Set the dispersion control on the RF section to 100Hz per division. Adjust the Fine Tuning control to center the display precisely. Set the bandwidth on the RF section to 10Hz. Set the sweep time on the IF section to 10 seconds per division. Set video filter (IF section) to 10Hz (or 1Hz if modified).
- . Place the sweep in the Single Sweep position and the display persistence to MAX. Press the single sweep button on the IF unit and observe the general appearance of the display.

- . Place the sweep control (IF unit) on manual and adjust the display so that it is exactly one division away from the carrier.
- . Increase the IF log reference level by 3 steps, to -40.

The top line of the display is now 30dB below the carrier. (CAUTION: Any further increase in log level can result in loss of sensitivity). The -50dB line is now -80dB relative to the carrier.

By switching the dispersion control (RF section) to 200, 500, 1000, 20,000, and 50,000Hz the noise level relative to the carrier at these offset frequencies can be measured.

Certain spectrum analyzers have been modified to have a video bandwidth (IF section) of 1Hz. This reduces the vertical spread of the noise display and makes the average noise power reading unambiguous. The vertical output of the spectrum analyzer can be externally filtered and displayed on an oscilloscope's CRT. The oscilloscope's vertical gain and position controls must be adjusted so the oscilloscope display tracks the spectrum analyzer display.

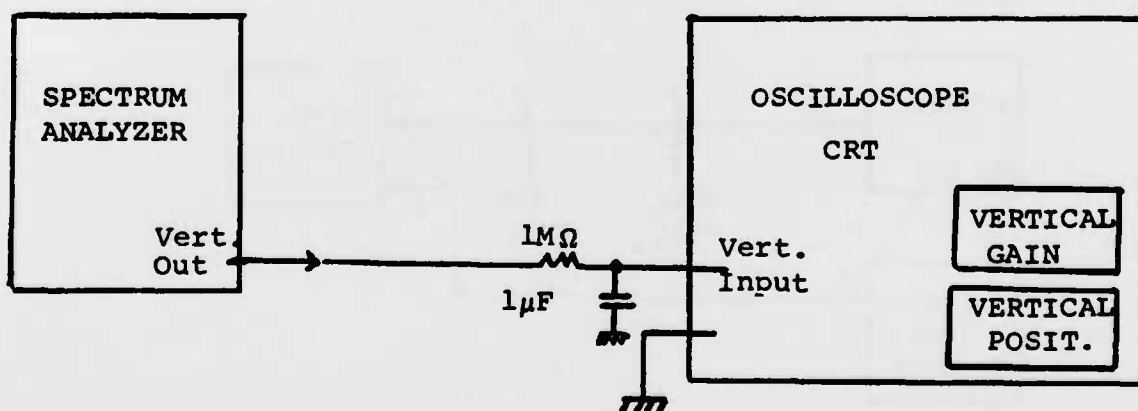


Figure 96. Oscilloscope Tracking Setup

<u>OFFSET FREQUENCY</u>	<u>SPEC IN 10Hz IF BW</u>
20Hz	-30dBc
200Hz	-70dBc
5000Hz	-80dBc
50000Hz	-90dBc

Record the test results on Table 14.

Spectral Purity: Discrete frequency components

#### 5.5.5 Low Frequency Components

- . Increase the IF log reference by 3 steps, to -40. The top line is now 30dB below the carrier.
- . Press the single sweep button and observe the display. Inspect display to detect if there are any low frequency components which miss the specification.

NOTE: All 60Hz spurious components were below the specifications.

#### 5.5.6 Other Discrete Components

Very low level discrete components are difficult to detect because they are surrounded by random noise. Their detection will be as follows:

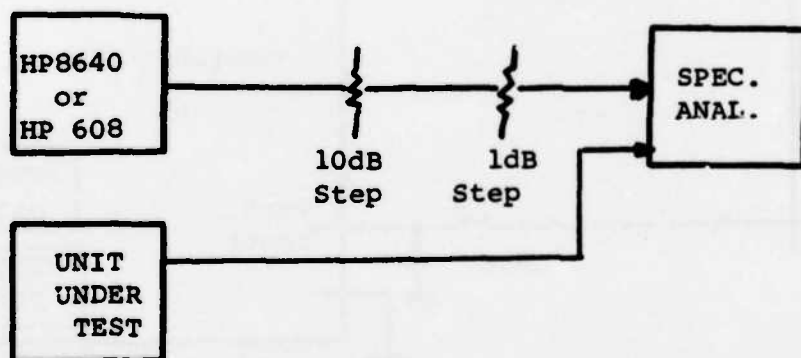
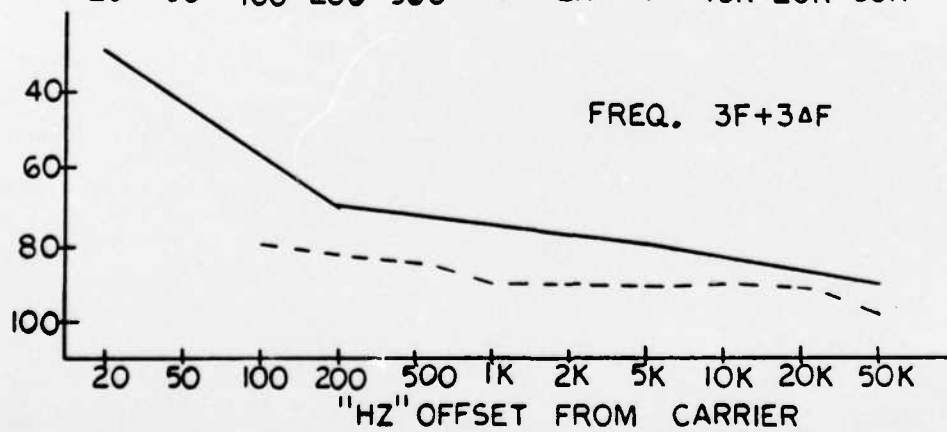
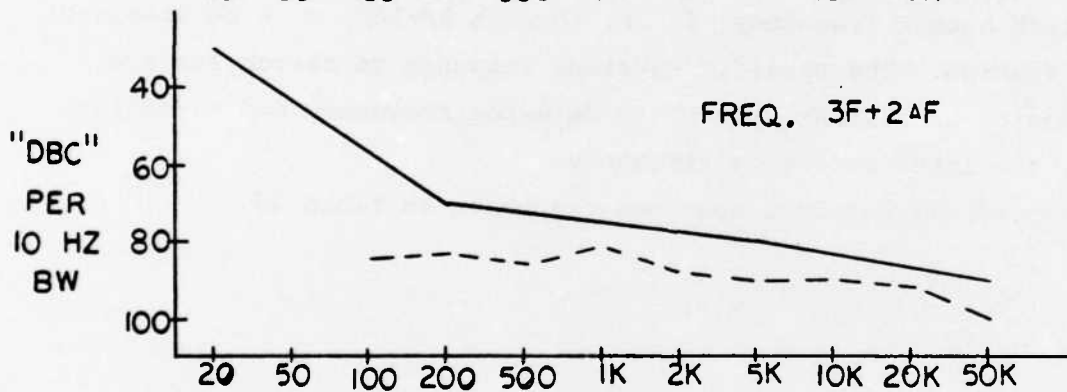
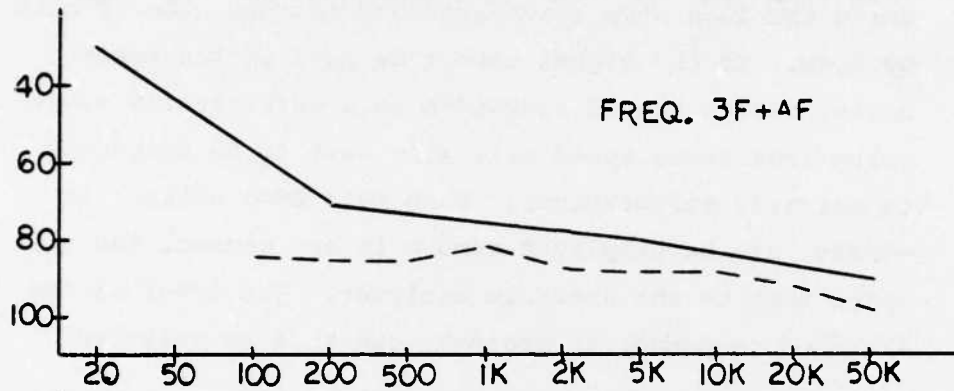
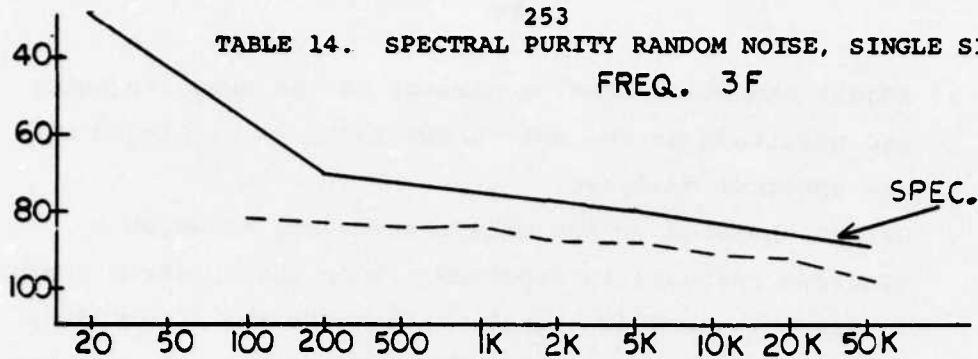


Figure 97. Discrete Component Spectral Response Test, Bench Test Setup

TABLE 14. SPECTRAL PURITY RANDOM NOISE, SINGLE SIDED  
FREQ.  $3F$



- . Adjust the 8640 signal generator to the same frequency and amplitude as the unit under test, as displayed on the spectrum analyzer.
- . Offset the 8640 by the offset frequency at which a spurious response is expected. Tune the spectrum analyzer to display the 8640 signal. Attenuate the signal 80dB using the 10dB step attenuator and increase the IF gain by 20dB. If the signal cannot be seen in the ambient noise, reduce the IF bandwidth to a sufficiently small value (The sweep speed will also have to be decreased to maintain calibration). When this 8640 signal, at -80dBc, can be displayed remove it and connect the unit under test to the spectrum analyzer. The level of the spurious response, if present, can thus be measured.

Each output frequency,  $f$ ,  $3F$ , through  $3F+3\Delta F$ , must be examined in this fashion. The specific spurious response to search for are the harmonics of 12.5KHz, the phase detector frequency and harmonics of 1MHz, the input reference frequency.

Record all detected spurious responses on Table 15.

TABLE 15. SPURIOUS RESPONSES (IN DB BELOW THE CARRIER) AT OFFSET FREQUENCIES WHICH ARE MULTIPLES OF THE PHASE DETECTOR.

	Output Frequency	$F$	$3F$	$3F+\Delta F$	$3F+2\Delta F$	$3F+3\Delta F$
$\Delta f_1 = 12.5 \text{ KHz}$	$-3\Delta f$	$<-90$	-90	-92	-90	-90
	$-2\Delta f$	-86	-86	-93	-87	-86
	$-1\Delta f$	-81	-84	-82	-82	-82
	$+1\Delta f$	-80	-82	-82	-82	-83
	$+2\Delta f$	-86	-87	-93	-88	-87
	$+3\Delta f$	$<-90$	-90	-92	-89	-90
$\Delta f_2 = 1 \text{ MHz}$	$-3\Delta f$		-94	-90	-91	-90
	$-2\Delta f$	-93	-94	-90	-91	-90
	$-1\Delta f$	-92	-93	-79	-92	-88
	$+1\Delta f$	-92	-93	-78	-91	-87
	$+2\Delta f$	-92	-94	-88	-92	-90
	$+3\Delta f$		-94	-91	-92	-91

Mutual leakage/coupling between output signals:

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Harmonics of output signals:

F output:

3F output:

3F+ F output:

3F+2 F output:

3F+3 F output:

## 5.6 OPERATION

To operate the reference generator, apply +12VDC (750ma) and -12VDC (60ma) and ground. The power supplies should be of good laboratory quality. Precautions should be taken to avoid ground loops. The reference generator should have its own set of wires to the +12 volt supplies instead of sharing a set with other equipments.

A 1MHz reference input of 0dBm (nominal) into 50 $\Omega$  should be tuned to within 0.1Hz or closer, dependent upon the output frequency error tolerated. The reference generator will lock up to a +1Hz mistuning at room temperature (70°F +30°F) and meet all specified goals. Not all (nominally) 1MHz system references are within the frequency accuracy demands of the synthesizer and, thus, the reference generator. Thus, before being connected to the reference generator, the system's 1MHz reference frequency should be adjusted for accuracy.

Although a 0dBm 1MHz sinewave is the expected input signal, the unit will accept a wide range of waveforms. The input power should be kept between -3dBm and +3dBm. Note that the 3F output is taken at the output of Unit 1. (Unit 2 which develops the 3F signal, drives Unit 1 which delivers 3F and F to the synthesizer.)

## 5.7 Maintenance

The reference generator requires only one maintenance adjustment which pertains to Units 2, 3, 4 and 5. The purpose of the adjustment is to compensate for crystal aging in the VCXO.

### Procedure

Detach Unit 2 from the reference generator chassis and remove cover. Disconnect no power wires or coax cables, but position the unit for access to its circuitry.

Turn the reference generator ON. Adjust the 1MHz reference so that the output of Unit 2 is within  $\pm 3.0\text{Hz}$  of its nominal frequency.

With a high impedance voltmeter (e.g., digital), measure the voltage at the junction of R1 and R2. This VCXO tuning voltage,  $V_T$ , should fall within the range of  $3.8\text{V} \leq V_T \leq 4.2\text{VDC}$  at room temperature,  $68^\circ\text{F}$ .

If  $V_T$  is outside of this range, then adjust C4 to bring  $V_T$  as close to 4.0VDC as possible.

Adjustment, if the phase-lock loop is not locked (such as after VCXO component replacement, subsequent to repair). Unsolder wire from phase detector to R1 of VCXO. Substitute a voltage of 4.0 VDC from a clean external power supply. Adjust C4 for a VCXO output frequency within  $\pm 3\text{Hz}$  of nominal. Reconnect the wire from the phase detector, U8 Pin 6, to R1 of the VCXO.

Either of these maintenance procedures should be performed three months after receipt of the reference generator (assuming it was left ON for most of that time) and at six months intervals thereafter.

## 5.8 CONCLUSIONS

The test results relating to spectral purity caused by random noise, indicate that the units under test surpass the goals by 5 to 22dB.

The smallest offset frequency which could be accommodated was 100 Hz. This limitation was imposed by the skirts of the spectrum analyzer's IF filter which passed enough carrier to sweep out any contribution of random noise to the display. Consequently, the specified point at 20 Hz offset could not be measured. Considering that, at 100 Hz, the noise is already 22dB less the specified goal, there is hardly a way that goal could be exceeded only 80 Hz away. Note also that the noise specification has been adjusted to reflect the 10 Hz bandwidth of spectrum analyzer, i.e. -80dB per Hz BW equals -70dB per 10 Hz BW, for random noise.

The test results for discrete spurious components indicate that all but one pair of discrete sidebands were down by at least 80dB, the requirement for this brassboard version of the reference generator. (The 1 MHz sidebands on the  $3F+\Delta F$  unit were down -78 and -79dB.)

Attainment of -100dBc discrete sideband performance from the frequency synthesizer requires the same performance from the reference generator. Brassboard packaging is not generally compatible with -100dBc performance. Achievement of such requires a unique package, designed and fabricated to provide optimal signal routing with low leakage and high isolation

between signals. Package improvement would, of course, allow the discrete sideband contributions of the internal circuitry, masked by the present brassboard packaging, to be eliminated through circuit re-layout or redesign. As the random phase noise characteristics of the present reference generator are already better than specified no improvement due to repackaging is expected.

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